GENERAL DESCRIPTION

The MXC3439ALA is a 3-axis MEMS accelerometer with a large feature set optimized for consumer product motion sensing. Applications include smartphones, user interface control, gaming motion input, game controllers, remote controls, and portable media products.

The MXC3439ALA features algorithms to support Any Motion/No Motion, Shake, Tilt/Flip and Tap/Double/Triple-Tap detection, 6D orientation, and Freefall detection.

Low power and low noise modes support a wide range of customer applications. A 32-sample FIFO supports data capture.

Two interrupt pins (INT1/INT2) can output any of 10 interrupt sources (sample, motion, FIFO) with selectable level and drive modes.

The MXC3439ALA is optimized for applications like smartphones, IOT, game controllers, and toys.

FEATURES

Range, Sampling & Power

- ±2, ±4, ±8, ±16g range
- 16-bit single sample resolution
- 16-bit resolution with 32-byte FIFO
- 1 to 1600 Hz Output Data Rate
- Typical active current
  - ✓ 1uA sleep mode
  - ✓ 10uA low power mode
  - ✓ 170uA low noise mode
- Full motion detection features

Simple System Integration

- SPI up to 10 MHz
- I2C interface, up to 1 MHz
- I3C interface, up to 12.5 MHz
- 2×2×0.93 mm 12-pin LGA package
- RoHS compliant

Applications

- Smartphones
- IOT Devices
- Game Controllers

Information furnished by MEMSIC is believed to be accurate and reliable. However, no responsibility is assumed by MEMSIC for its use, or for any infringements of patents or other rights of third parties which ay result from its use. No license is granted by implication or otherwise under any patent or patent rights of MEMSIC.

© MEMSIC Semiconductor (Tianjin) Co., Ltd.

www.memsic.com

TABLE OF CONTENTS

1. Order Information 6
2. Functional Block Diagram 7
3. Packaging and Pin Description 8
   3.1 Package Outline 8
   3.2 Package Orientation 9
   3.3 Pin Description 10
   3.4 Typical Application Circuits 11
      3.4.1 I2C Application Circuit 11
      3.4.2 I3C Application Circuit 12
      3.4.3 SPI Application Circuit (4-wire) 13
      3.4.4 SPI Application Circuit (3-wire) 14
   3.5 Tape and Reel 15
   3.6 Soldering Profile 17
   3.7 Shipping and Handling Guidelines 17
   3.8 Moisture Sensitivity Level Control 17
4. Specifications 18
   4.1 Absolute Maximum Ratings 18
   4.2 Sensor Characteristics 19
   4.3 Electrical Characteristics 20
   4.4 Communication Interface Characteristics 21
      4.4.1 SPI - Serial Peripheral Interface 21
      4.4.2 I2C Communications Interface 24
      4.4.3 I3C Communications Interface 26
5 General Operation 28
   5.1 Operating Modes 29
6 Registers 30
   6.1 Register Descriptions 30
      6.1.1 0x00 - Chip ID Register 30
      6.1.2 0x01 - Version Register 30
      6.1.3 0x02 – Power Control/Reset Register 31
      6.1.4 0x03 – Device Status Register 32
      6.1.5 0x04 – Control Register 1 33

MEMSIC

6.1.6 0x05 – Control Register 2 37
6.1.7 0x06 – Control Register 3 40
6.1.8 0x07 – Control Register 4 42
6.1.9 0x08 to 0x0D – XL Output Registers 43
6.1.10 0x0E, 0x0F – Temperature Output Data 44
6.1.11 0x10, 0x11 – Interrupt Status and Clear Registers 1/2 45
6.1.12 0x12 – Sensor and Motion Status Register (Status Register) 47
6.1.13 0x13 – FIFO Control Register 1 48
6.1.14 0x14 – FIFO Control Register 2 49
6.1.15 0x15 – FIFO Control Register 3 50
6.1.16 0x16 – FIFO Status Register 1 51
6.1.17 0x17 – FIFO Status Register 2 52
6.1.18 0x18 – FIFO Status Register 3 53
6.1.19 0x19 to 0x1E – FIFO_DOUT Registers 54
6.1.20 0x1F - ODR Divide Register 55
6.1.21 0x20 – ODR Prescale Register 56
6.1.22 0x21 – TEMP Control 57
6.1.23 0x22 – XL XY Decimation Register 58
6.1.24 0x23 – Interrupt Control Register 0 59
6.1.25 0x24 – Interrupt Control Register 1 60
6.1.26 0x25 – Interrupt Control Register 2 61
6.1.27 0x26 – INT Pad Control Register 62
6.1.28 0x27 – GPIO Control Register 63
6.1.29 0x28 – I3C Parameter Register 1 65
6.1.30 0x29 – I3C Parameter Register 2 66
6.1.31 0x2A – I3C Parameter Register 3 67
6.1.32 0x2B,0x2C – AnyMotion Motion Delta Threshold 68
6.1.33 0x2D – AnyMotion Duration Threshold 69
6.1.34 0x2E – AnyMotion Control Register 0 70
6.1.35 0x2F – Motion Control Register 1 71
6.1.36 0x30 – Motion Control Register 2 72
6.1.37 0x31,0x32 – Tilt/Flip Threshold Register 73

MEMSIC

6.1.38 0x33 – Tilt/Flip Debounce Register 74
6.1.39 0x34,0x35 – NoMotion Threshold Register 75
6.1.40 0x36 – NoMotion Debounce Register 76
6.1.41 0x37,0x38 – Shake Threshold Register 77
6.1.42 0x39,0x3A – Shake Peak 2 Peak Duration Threshold Register 78
6.1.43 0x3B,0x3C – TAP Event Threshold Register 79
6.1.44 0x3D – TAP Shock Duration Register 80
6.1.45 0x3E – TAP Quiet Duration Register 81
6.1.46 0x3F – TAP Latency Duration Register 82
6.1.47 0x40 – TAP Control Register 83
6.1.48 0x41,0x42 – Freefall Threshold Register 84
6.1.49 0x43 – Freefall Duration Register 85
6.1.50 0x44,0x45 – Six Degrees High Threshold Register 86
6.1.51 0x46,0x47 – Six Degrees Low Threshold Register 87
6.1.52 0x48 – Six Degree Duration Register 88
6.1.53 0x49 – Six Degrees Status Register 89
6.1.54 0x4A – Pipeline Status Register 90
6.1.55 0x4E-0x55 – XY Axis LPF Coefficients 91
6.1.56 0x56 – Pipeline Control Register 92
6.1.57 0x58 - 0x5D – XL Offset_0 Registers 93
6.1.58 0x5E - 0x61,0x6C,0x79 – XL Offset_1 Registers 94
6.1.59 0x62 – XL Polarity Register 95
6.1.60 0x63-0x69 – XL AOFS Offset Registers 96
6.1.61 0x6A,0x6B – XL Analog Gain Register 1 and 2 97
6.1.62 0x6D-0x72 – TCO Coefficient Registers 100
6.1.63 0x73-0x78 – TCS Coefficient Registers 102
6.1.64 0x7A,0x7B,0x7C,0x7D – Temperature Trim Registers 105
6.1.65 0x7E,0x7F,0x80 - Pre-Digital Gain Registers 107
6.1.66 0x81,0x82 - SYS_OSC Trim Registers 1/2 108
6.1.67 0x84 - 0x87 – Device ID/Part ID Registers 109
6.1.68 0x88 - Analog Control Register 1 110
6.1.69 0x8C – Analog Control Register 5 111

MEMSIC

6.1.70 0x8D – Analog Control Register 6 112
6.1.71 0x90 – Z-Axis Decimation Count 113
6.1.72 0x91 – Z-Axis Control Register 114
6.1.73 0x92 – Self-Test Hold Count Register 115
6.1.74 0x94 – Digital Test Register 2 (Self-Test Count) 116
6.1.75 0x95 – Warm-up Register (SDM Power Delay Count) 117
6.1.76 0x98 – SINC Dummy Count Register 118
6.1.77 0x9C – XL Self-Test Register 2 119
6.1.78 0x9D – XL SINC State FSM Status Register 121
6.1.79 0xA0, 0xA1 – XY Axis DCM Test Registers 122
6.1.80 0xA2 – Interrupt Auto Clear Register 123
6.1.81 0xA4,0xA5 – Z Axis DCM Test Registers 125
6.1.82 0xA9,0xAA – Temperature Calibration Output Registers 126
6.1.83 0xAB,0xAC – Self Test Threshold Registers 128
6.1.84 0xAD-0xB4 – Z Axis LPF Coefficients 129
7 List of Tables 130
8 List of Figures 133
9 Revision History 134
10 Legal 135

MEMSIC

1. ORDER INFORMATION

Part Number	Resolution	Order Number	Package	Tape & Reel
MXC3439ALA	16bit	MXC3439ALA	LGA-12L	10Ku

Table 1: Order Information



Row	Marking
B	Device Code
XX	Trace Code
CC	Factory Lot Code
●	Pin1 Identifier

Table 2: Package Information

MEMSIC

2. FUNCTIONAL BLOCK DIAGRAM

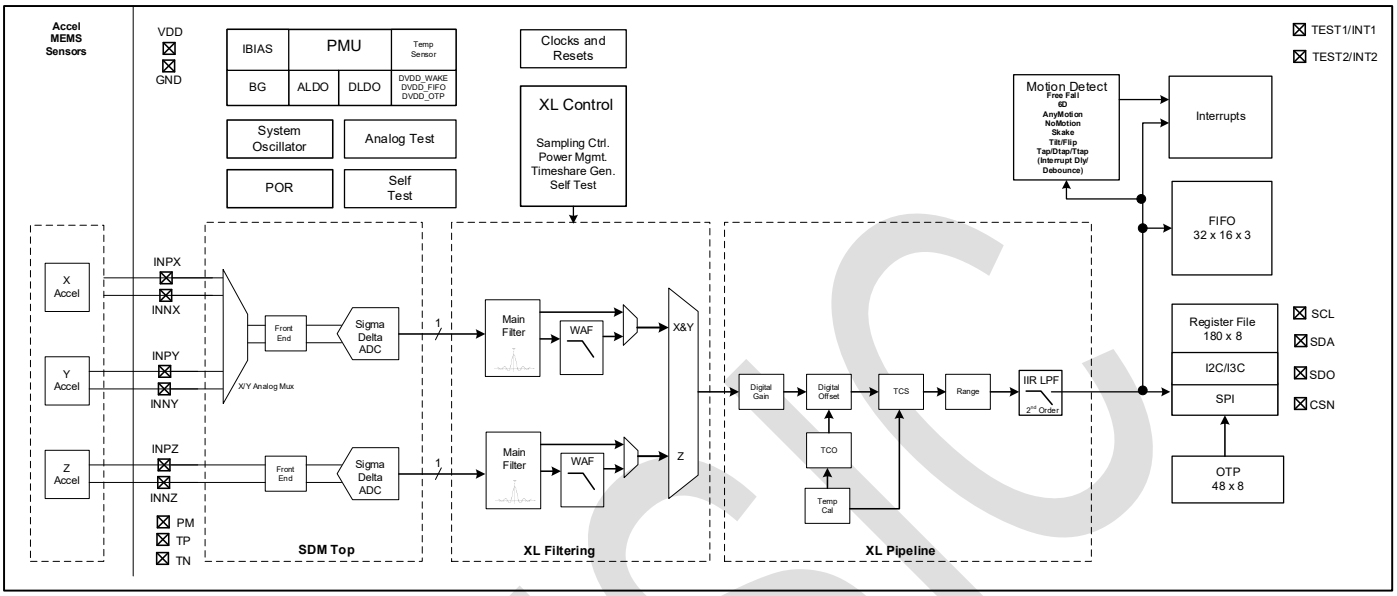
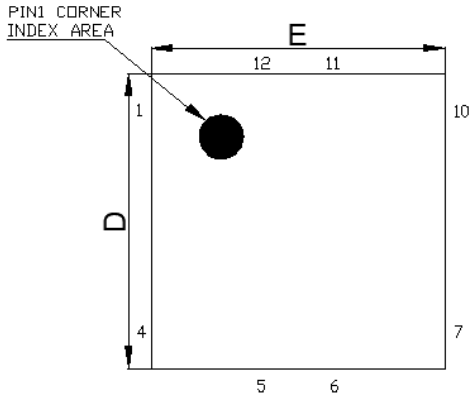


Figure 1: Block Diagram

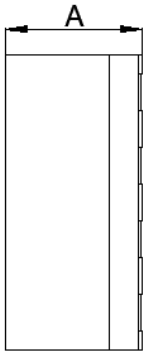
MEMSIC

3. PACKAGING AND PIN DESCRIPTION

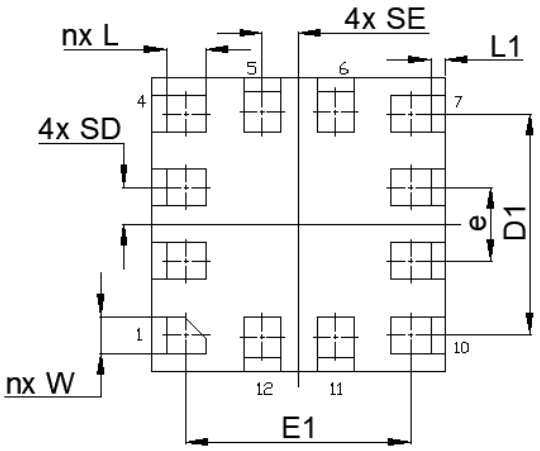
3.1 PACKAGE OUTLINE



Top view



Side view



Bottom view

	SYMBOL	DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.88	0.93	0.98
BODY SIZE	D	1.95	2.00	2.05
	E	1.95	2.00	2.05
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.225	0.275	0.325
BODY EDGE TO LEAD EDGE	L1	0.050	0.100	0.150
LEAD COUNT	n	12		
LEAD PITCH	e	0.5 BSC		
EDGE LEAD CENTER TO CENTER	D1	1.5 BSC		
	E1	1.525 BSC		
BODY CENTER TO CONTACT LEAD CENTER	SD	0.25 BSC		
	SE	0.25 BSC		

Figure 2: Package Outline and Mechanical Dimensions

3.2 PACKAGE ORIENTATION

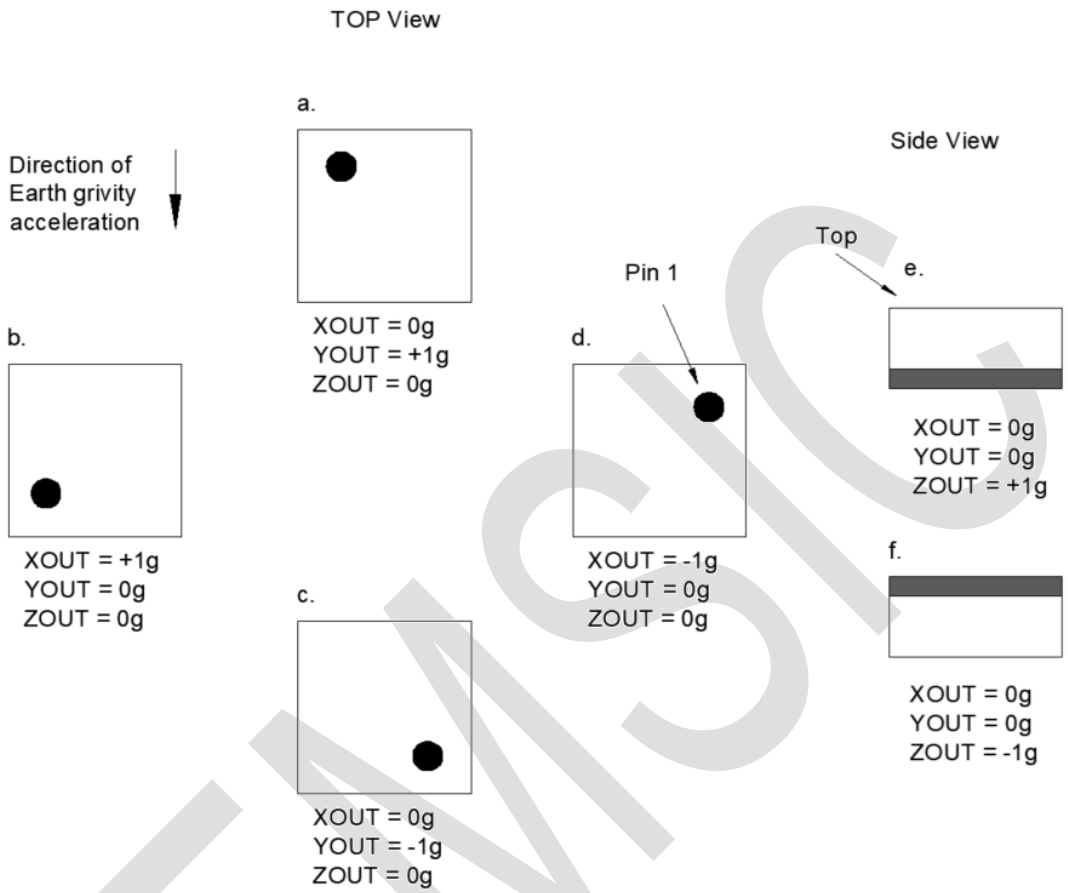


Figure 3: Package Orientation

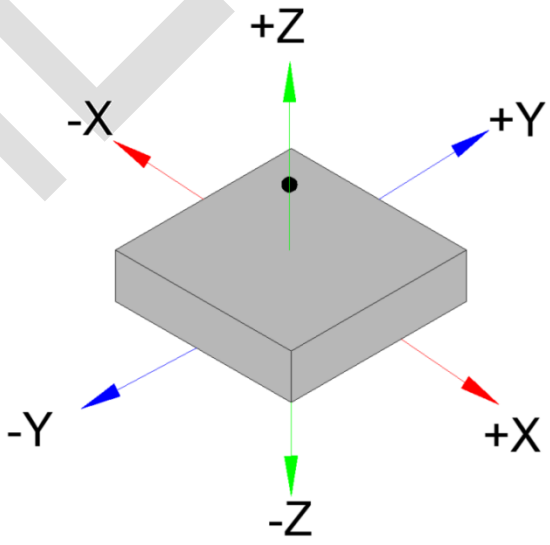
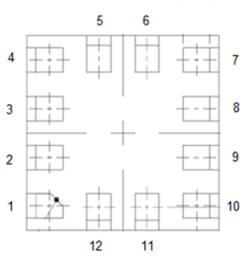


Figure 4: Package Axis Reference

MEMSIC

3.3 PIN DESCRIPTION



(Bottom View)

Pin	Name	Function
1	SDO/DOUT_A6	SPI data output (MISO) Address select in I2C mode
2	SDI/SDA[1]	SPI data In (MOSI) I2C serial data input/output
3	VDDIO	Power supply for interface
4	NC[4]	NC[4]
5	INT1[2]	Interrupt active LOW [3]
6	INT2[2]	Interrupt active LOW [3]
7	VDD	Power supply for internal
8	NC[4]	NC[4]
9	GND	Ground
10	CSN	Chip select for SPI (active low) **I2C must connect to VDD**
11	NC[4]	NC[4]
12	SCK/SCL[1]	SPI/I2C serial clock

Table 3: Pin Description

Notes:

1) SCL and SDA require a pull-up resistor, typically 4.7kΩ to pin VDD. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.

2) INT1/2 pins can be configured by software to operate either as an open-drain output or push-pull output (mode register). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to VDDIO or VDD.

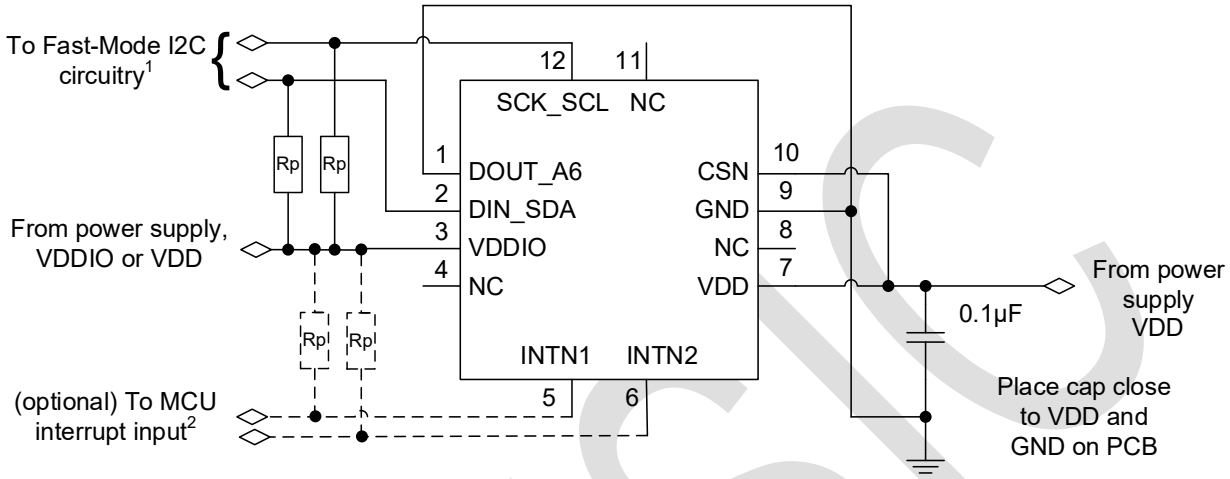
3) INT1/2 pin polarity is programmable in the pad control register.

4) NC or “no connect” pins do not have any function on the MXC3439ALA, and may be left unconnected, tied to GND, or tied to VDD.

MEMSIC

3.4 TYPICAL APPLICATION CIRCUITS

3.4.1 I2C APPLICATION CIRCUIT



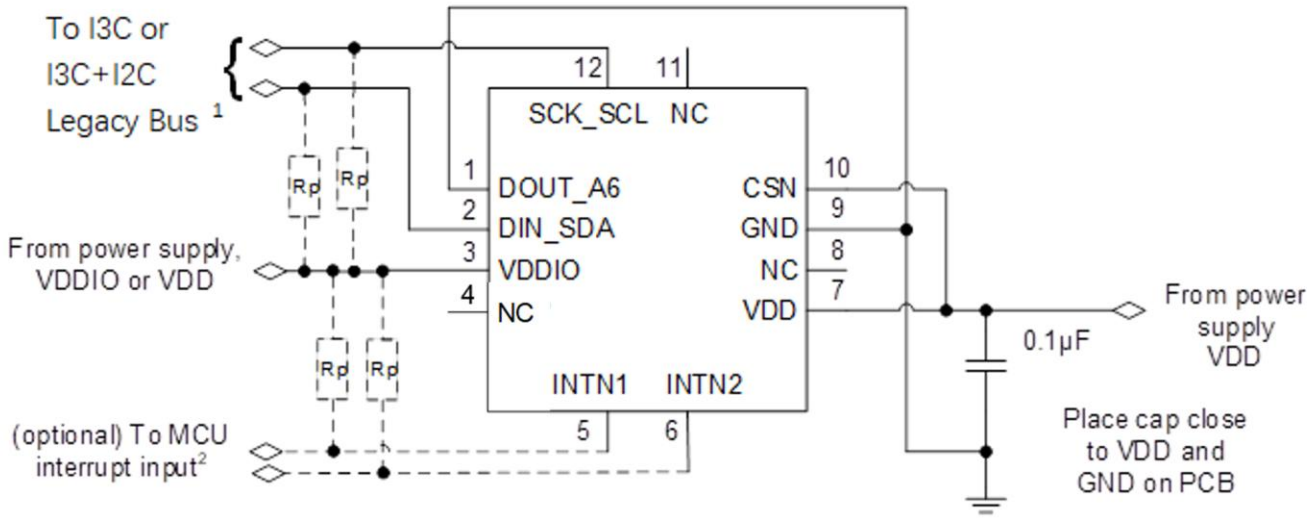
NOTE[1]: Rp are typically 4.7kΩ pullup resistors to VDDIO, per I2C specification. When VDDIO is powered down, DIN_SDA and SCK_SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 5: Typical I2C Application Circuit

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the VDD pin.

MEMSIC

3.4.2 I3C APPLICATION CIRCUIT



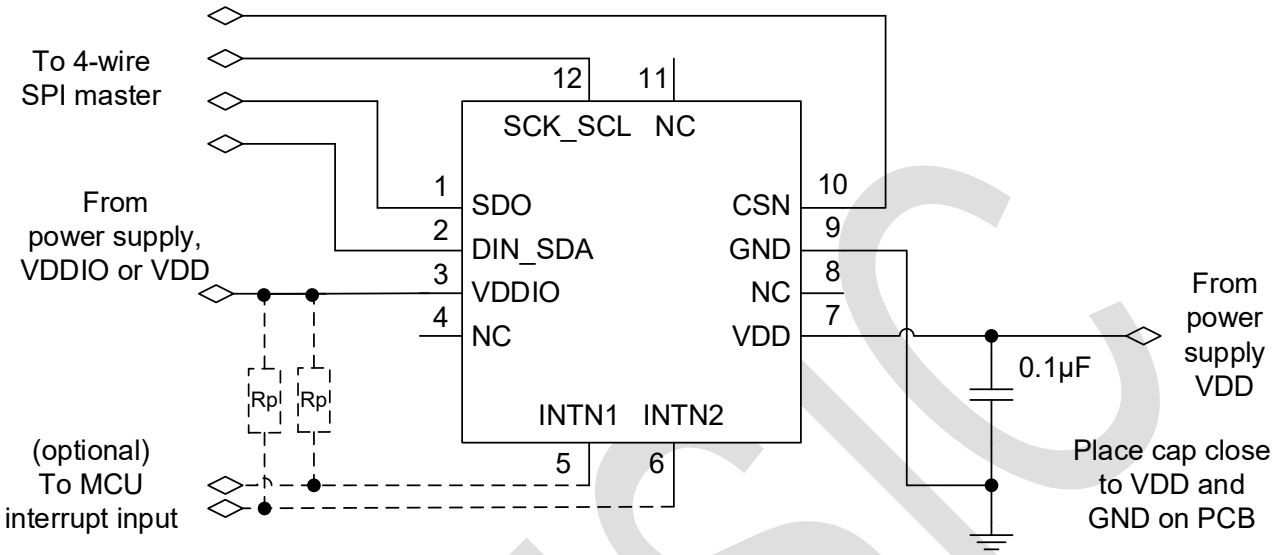
NOTE[1]: For I2C+I3C open-drain operations, 1.1 k pullup resistors to VDDIO recommended.

NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 6: Typical I3C Application Circuit

MEMSIC

3.4.3 SPI APPLICATION CIRCUIT (4-WIRE)

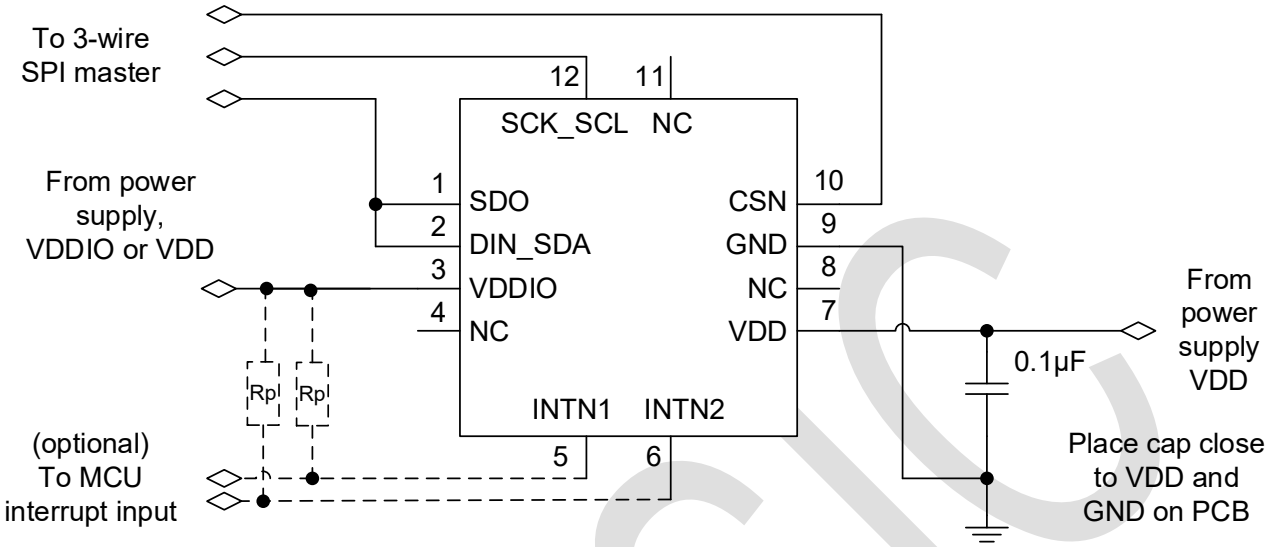


NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 7: Typical 4-wire SPI Application Circuit

MEMSIC

3.4.4 SPI APPLICATION CIRCUIT (3-WIRE)



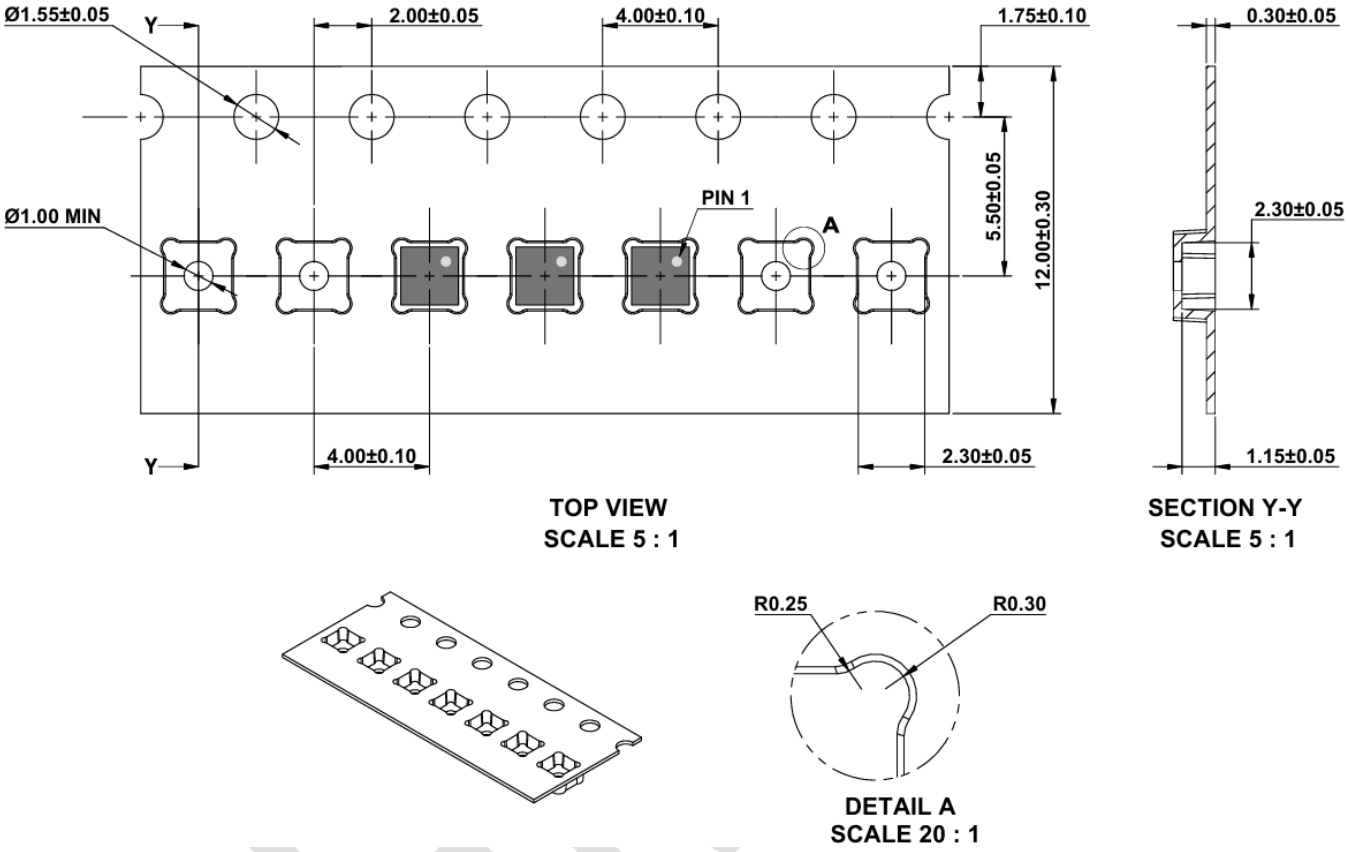
NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 8: Typical 3-wire SPI Application Circuit

MEMSIC

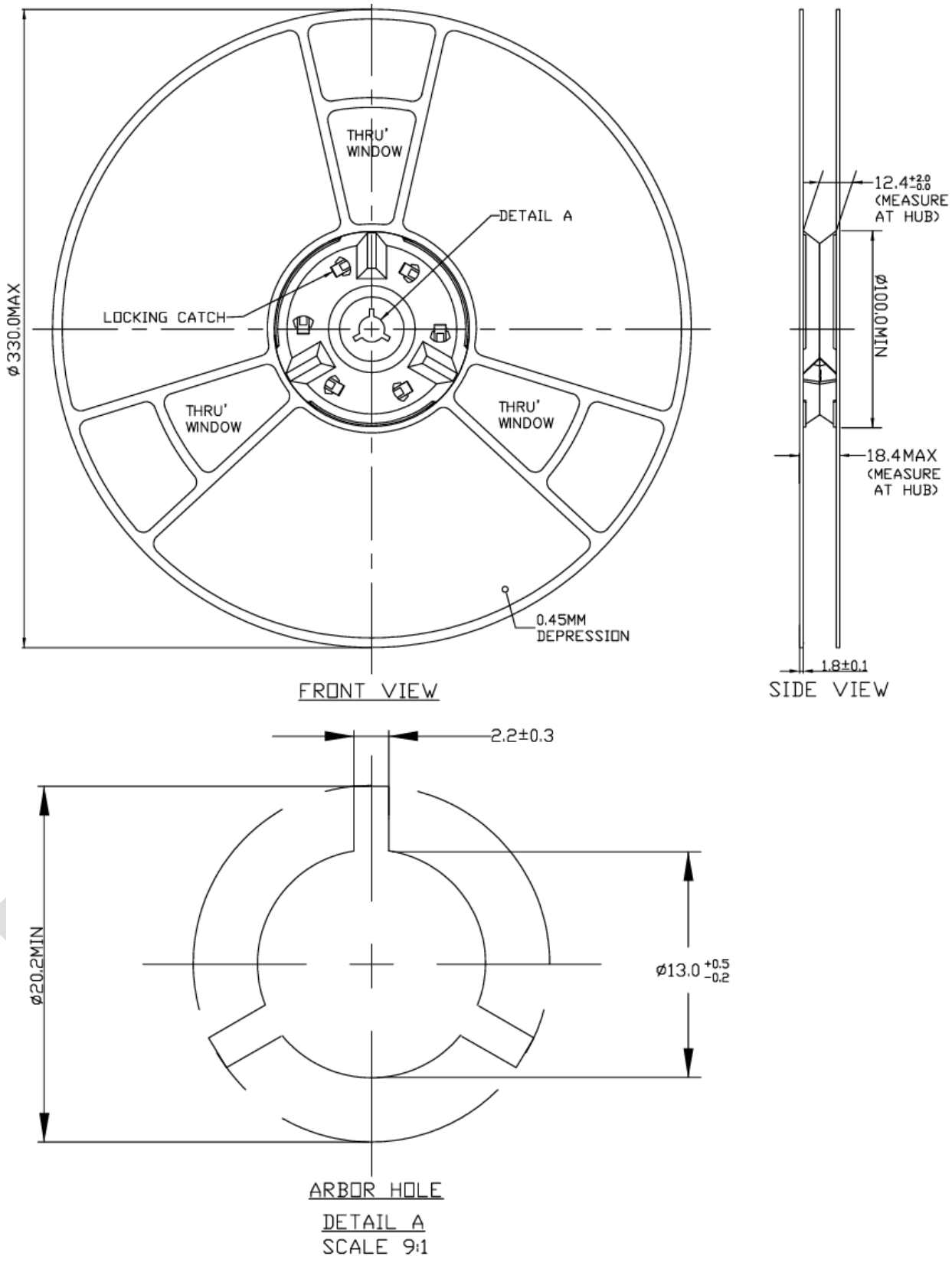
3.5 TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See **Figure 9: Tape Dimensions** and **Figure 10: Reel Dimensions**.



- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ±0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 9: Tape Dimensions



- Dimensions in mm.

Figure 10: Reel Dimensions

3.6 SOLDERING PROFILE

The LGA package follows the reflow soldering classification profiles described in *Joint Industry Standard, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*, document number J-STD-020E. Reflow soldering has a peak temperature (T_p) of 260ºC

3.7 SHIPPING AND HANDLING GUIDELINES

Shipping and handling follow the standards described in *Joint Industry Standard, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*, document number J-STD-033C.

The following are additional handling guidelines (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- While the mechanical sensor is designed to handle high-g shock events, direct mechanical shock to the package should be avoided.
- SMT assembly houses should use automated assembly equipment with either plastic nozzles or nozzles with compliant tips (for example, soft rubber or silicone).
- Avoid g-forces beyond the specified limits during transportation.
- Handling and mounting of sensors should be done in a defined and qualified installation.

3.8 MOISTURE SENSITIVITY LEVEL CONTROL

The moisture sensitivity level is 1 for this product. The following are storage recommendations (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- Store the tape and reel in the *unopened* dry pack, until required on the assembly floor.
- If the dry pack has been opened or the reel has been removed from the dry pack, reseal the reel inside of the dry pack with a black protective belt. Avoid crushing the tape and reel.
- Store the cardboard box in a vertical position.

MEMSIC

4. SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Parameter	Condition	Minimum	Maximum	Unit
Supply Voltages	VDD/VDDIO	-0.3	+3.6	V
Ambient operating temperature	T_{OP}	-40	+85	ºC
Storage temperature	T_{STG}	-40	+125	ºC
Mechanical Shock	Duration ≤ 200 µs	-	10,000	g
	Duration ≤ 1.0ms	-	3,000	g
ESD	HBM	± 2000	-	V
	CDM	± 500	-	V
Latch-up current at T_{op} = 25 ºC	I_{LU}	-	100	mA

Table 4: Absolute Maximum Ratings

MEMSIC

4.2 SENSOR CHARACTERISTICS

Specifications based on the following conditions: VDD/VDDIO 1.8V, ODR 100Hz, and T = 25°C unless stated otherwise.

Parameter	Conditions		Min	Typ	Max	Unit
Accel FSR	Selectable			±2/4/8/16		g
Sensitivity	FSR = ±2.0g			16384		LSB/g
	FSR = ±4.0g			8192		
	FSR = ±8.0g			4096		
	FSR = ±16.0g			2048		
Sensitivity error				±1		%
Sensitivity Temperature Coefficient(1)	-40≤ Top ≤ +85 ^{0}C			±0.025		%/^{0}C
Zero-g Offset	Chip Level			±40		mg
	Board Level			±80		
Zero-g Offset Temperature Coefficient(1)	-40 ~ 85°C Board Level			±1		mg/°C
Noise Density	Chip Level (High performance)			X/Y=150 Z=240		μg/√Hz
RMS Noise	Chip Level (low power mode, ODR=50Hz)			6		mg
Nonlinearity (1)	FSR = ±2.0g			0.6		%FS
Cross-axis Sensitivity (1)	Between any two axes			±2		%
Output Data Rate			1		1600	Hz

1 Values are based on device characterization, not tested in production.

Table 5: Accel Sensor Characteristics

MEMSIC

4.3 ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage (VDD)	Rise-time<30mSec	1.71	1.8	3.6	V
Supply for IO (VDDIO)		1.08	1.2	VDD	V
Sleep current			1.5		μA
Current consumption	High performance mode (1600 Hz)		170		μA
	Low-power mode (100Hz)		10		μA
Startup Time (Boot to Ready)	VDD > 1.71V		3		ms
Start-up time			3		ms
Low-level output voltage (Vol)	SDO, INT1 or INT2, Iol < 2mA	0	-	0.3*VDDIO	V
High-level output voltage (Voh)	SDO, INT1 or INT2, Iol < 2mA	0.7*VDDIO	-	VDDIO	V
Operating temperature range		-40		85	°C

Table 6: Electrical Characteristics

MEMSIC

4.4 COMMUNICATION INTERFACE CHARACTERISTICS

4.4.1 SPI - SERIAL PERIPHERAL INTERFACE

The device always operates as an SPI slave. An SPI master must initiate all communication and data transfers and generate the SCK_SCL clock that synchronizes the data transfer. The CSN pin must be pulled up to VDDIO when the SPI interface is not in use. The SPI interface can operate in 3-wire or 4-wire mode (default). To enable 3-wire mode, connect the SPI DIN pin to the SPI DOUT pin on the PCB.

4.4.1.1 SPI PROTOCOL

The general protocol for the SPI interface is shown in the figure below. **Each transaction requires a minimum of 24 cycles of the SPI_CLK.** The falling edge of SPI_CS initiates the start of the SPI bus cycle. When the SPI master is writing data to MXC3439ALA via the SPI_DIN pin, data may change when the SPI_CLK is low and must be stable on the rising edge. Similarly, output data written from MXC3439ALA to the SPI master is shifted out on the SPI_DOUT pin on the falling edge of SPI_CLK and can be latched by the master on the rising edge of SPI_CLK. Serial data in or out of the device is always MSB first.

A total of 8-address bits is required for each SPI bus cycle. The first byte of the transaction is the command/address byte. During clock ‘1’, the R/W# bit is set to ‘0’ for a write cycle or ‘1’ for a read cycle. Clocks 2 to 8 specify the address to be written to or read from. Following clock 8, clocks 9-16 shift in the second address byte where clock 9 is address bit A7. Any clocks following 16 are for writing or reading data.

When the SPI master is writing data, data may change when the clock is low, and must be stable on the clock rising edge. Similarly, output data written to the SPI master is shifted out on the falling edge of clock and can be latched by the master on the rising edge of the clock. Serial data in or out of the device is always MSB first.

4.4.1.2 SINGLE REGISTER WRITE

A single register write consists of a 24 (one byte address) clock transaction. As described above, the first bit is set to ‘0’ indicating a register write followed by the register address. The 8th address bit A7 is at bit 9 of the transaction.

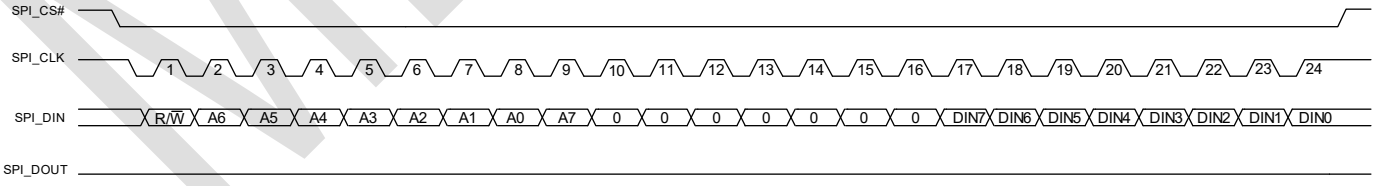


Figure 11: SPI single register write cycle

4.4.1.3 BURST REGISTER WRITE

A burst or multi-byte register write cycle uses the address specified at the beginning of the transaction as the starting register address. Internally the address will auto-increment to the next consecutive address for each additional byte (8-clocks) of data written beyond clock 24.

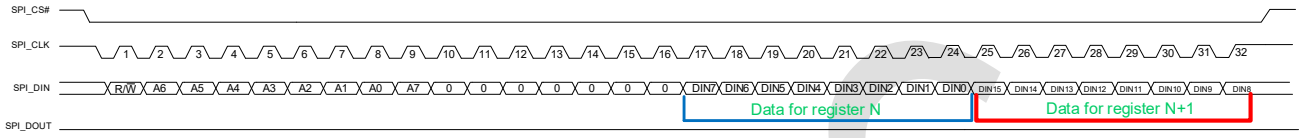


Figure 12: SPI Burst register write cycle (2 registers)

4.4.1.4 SINGLE REGISTER READ

A single register write consists of a 24 (two-byte address) clock transaction. As described above, the first bit is set to '1' indicating a register write followed by the register address.

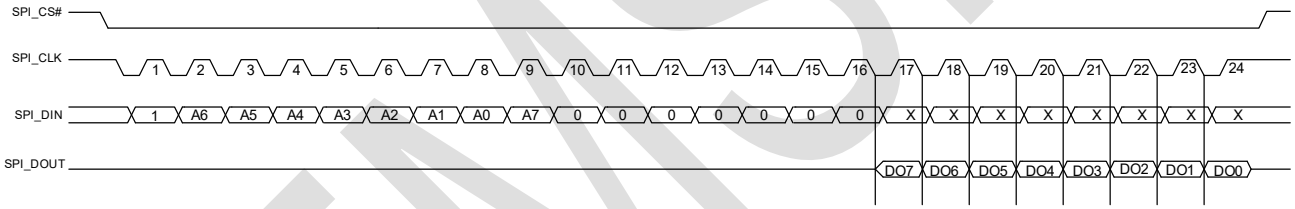


Figure 13: SPI single register read cycle

4.4.1.5 BURST REGISTER READ

A burst or multi-byte register read cycle uses the address specified at the beginning of the transaction as the starting register address. Internally the address will auto-increment to the next consecutive address for each additional byte (8-clocks) of data read beyond clock 24.

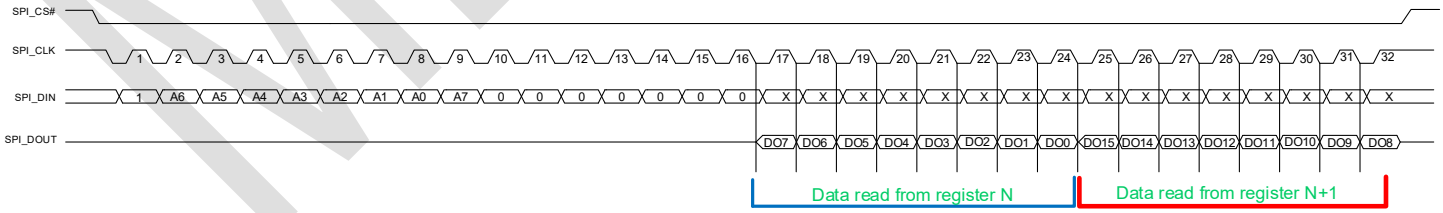


Figure 14: SPI Burst register read cycle (2 registers)

MEMSIC

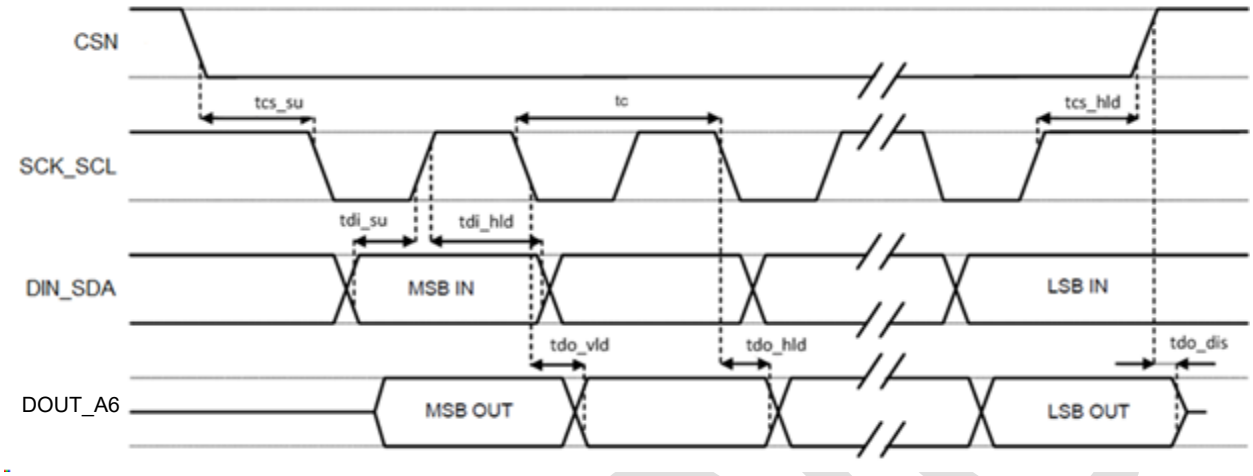


Figure 15: SPI Timing Waveform

Symbol	Parameter	Value		Units
		Min	Max	
tc	SPI SCK_SCL Clock Cycle	100		ns
fc	SPI SCK_SCL Clock Frequency		10	MHz
tcs_su	SPI CSN Setup Time	6		ns
tcs_hld	SPI CSN Hold Time	8		ns
tdi_su	SPI DIN_SDA Input Setup Time	5		ns
tdi_hld	SPI DIN_SDA Input Hold Time	15		ns
tdo_vld	SPI DOUT_A6 Valid Output Time		50	ns
tdo_hld	SPI DOUT_A6 Output Hold Time	9		ns
tdo_dis	SPI DOUT_A6 Output Disable Time		50	ns

Table 7: SPI Timing Parameters

4.4.2 I2C COMMUNICATIONS INTERFACE

The I2C device address depends upon the state of the SDO pin during power-up as shown in the table below.

7-bit Device ID	8-bit Address - Write	8-bit Address - Read	SDO level upon power-up
0x4C (7'b1001100)	0x98	0x99	GND
0x6C (7'b1101100)	0xD8	0xD9	VDD

Table 8: I2C Address Selection

I2C/I3C target operating in I2C mode only. Timing is based on the I2C specification and not tested in production.

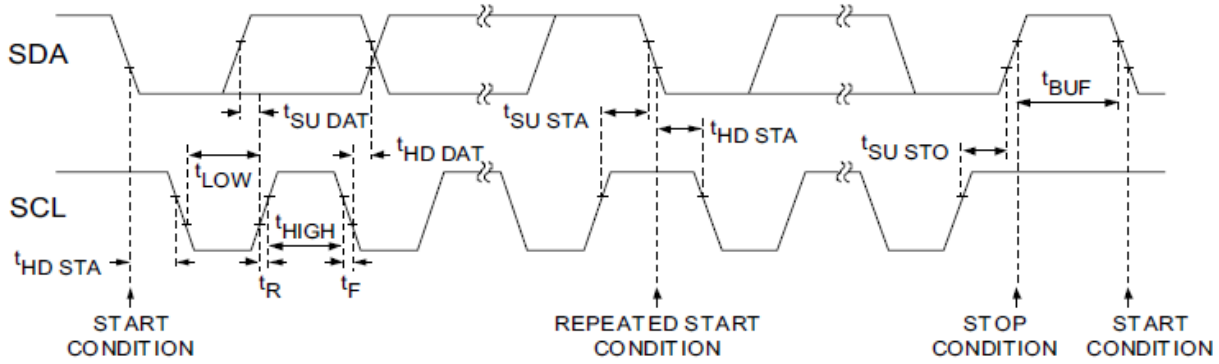


Figure 16. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	Data hold time [1]	0[2]	- [3]	0[2]	- [3]	0.9	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	50	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	0.5	-	µs

Table 9: I2C Timing Characteristics

1. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
2. A device must provide a hold time of at least 300 ns for the SDA signal (with respect to the Vih(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock. (Note $t_{VD;DAT}$(max) = $t_{VD;ACK}$(max) are 3.45 µs and 0.9 µs for Standard-mode and Fast-mode). Refer to the I2C Specification for more information.

MEMSIC

4.4.3 I3C COMMUNICATIONS INTERFACE

I2C/I3C target operating in I3C mode only.

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Input Low Level	V_{IL}		-0.5		0.3* V_{IO}	V
Logic Input High Level	V_{IH}		0.7*V_{IO}		V_{IO}	V
Hysteresis of Schmitt input	V_{hys}		0.2			V
Logic Output Low Level	V_{OL}				0.3* V_{IO}	V
Input Leakage Current	I_i	0.1V_{IO}<V_{in}<0.9V_{IO}	-10		10	μA
SCL Clock Frequency	f_{SCL}		0.01		7	MHz
START Hold Time	$t_{HD;STA}$		38.4			ns
START Setup Time	$t_{SU;STA}$		19.2			ns
LOW period of SCL	t_{LOW}		33			ns
HIGH period of SCL	t_{HIGH}		33			ns
Data Hold Time	$t_{HD;DAT}$		0		24	ns
Data Setup Time	$t_{SU;DAT}$		3			ns
Rise Time	t_r	From V_{IL} to V_{IH}			12	ns
Fall Time	t_f	From V_{IH} to V_{IL}			12	ns
Clock in to data out	tsco				12	ns
Bus Free Time Between STOP and START	t_{BUF}		1.3			μs
STOP Setup Time	$t_{SU;STO}$		19.2			ns

Table 10: I3C Timing Parameters

MEMSIC

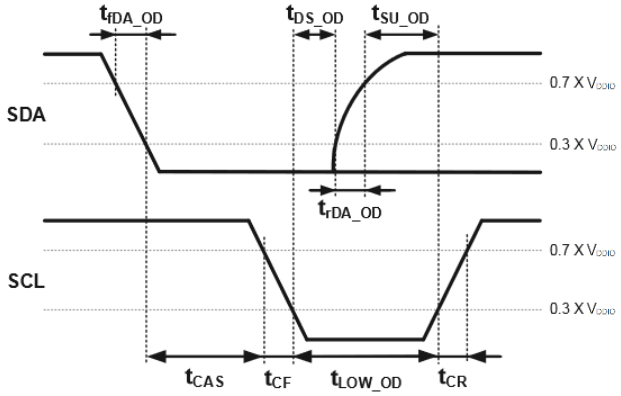


Figure 17: I3C START Condition Timing

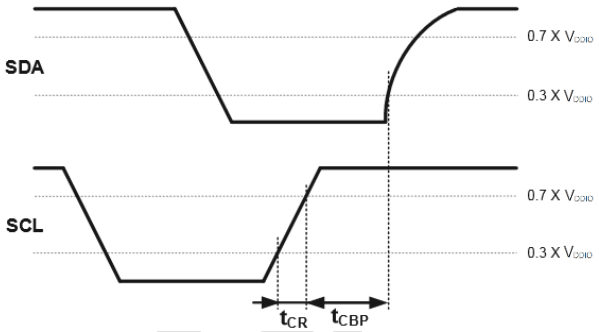


Figure 18: I3C STOP Condition Timing

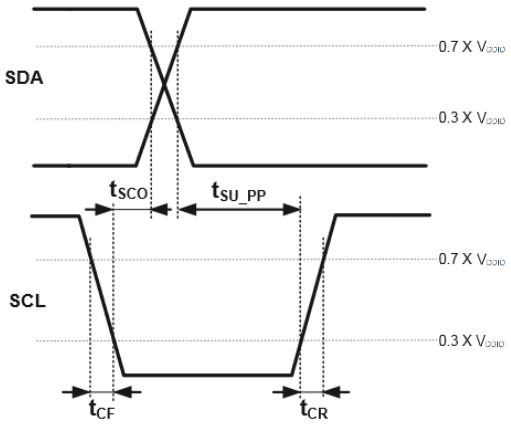


Figure 19: I3C Target Out Timing

5 GENERAL OPERATION

The MXC3439ALA is a three-axis MEMS accelerometer. supports low power and low noise operational modes. The MXC3439ALA communicates with the MPU/MCU through I2C (1 MHz), I3C (12.5 MHz), or SPI (10 MHz).

The MXC3439ALA features a motion block which implements algorithms to support many detection features such as “Any-Motion”, “No-Motion”, “Shake”, “Tilt/Flip”, “Tap/Double Tap/Triple Tap”, “6D Orientation”, and “Freefall”. The MXC3439ALA has two external interrupt pins (INT1, INT2). Any interrupt source may be assigned to either pin.

I2C Address:

7-bit Device ID	8-bit Address – Write	8-bit Address – Read	DOUT_A6 level upon power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDD

Table 11: I2C Address Selection

MEMSIC

5.1 OPERATING MODES

The device has three states of operation: SLEEP, STANDBY, WAKE (Low power mode and High-performance mode). All states are controlled by the software, there is no automatic power control.

The device defaults to the SLEEP state following a power-up and must be in the WAKE state before executing a reset.

The time to change from the STANDBY to WAKE state takes one sample period (takes less than 10 µs).

State	I2C/I3C/SPI Bus	Description
SLEEP	R/W	• Internal clocking is halted • No motion detection, sampling, or calibration • The I2C/I3C/SPI bus can read and write to registers (resolution, range, thresholds and other settings can be changed) • Reset not allowed • Default state after a power-up
STANDBY	R/W	• Internal clocking is enabled • No motion detection, sampling, or calibration • The I2C/I3C/SPI bus can read and write to registers (resolution, range, thresholds and other settings can be changed) • Reset allowed
WAKE	R	• WAKE mode ➢ Low power mode. ➢ High-performance mode: Highest power consumption. • Internal clocking is enabled • Continuous motion detection and sampling; automatic calibration is available • The I2C/I3C/SPI bus can only write to the mode register and read all other registers • Reset allowed

Table 12: Operating Modes

MEMSIC

6 REGISTERS

6.1 REGISTER DESCRIPTIONS

The resister set is accessed by the I2C, I3C or SPI interfaces.

6.1.1 0X00 - CHIP ID REGISTER

The Chip ID register returns the value of 0xFA.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x00	Chip ID Register CHIPID_REG	CHIP_ID[7:0]								0xFA	RO

6.1.2 0X01 - VERSION REGISTER

The Version ID register contains the current revision code of the MXC3439ALA.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x01	Version ID Register VERID_REG	VER_ID[7:0]								0x00	RO

MEMSIC

6.1.3 0X02 – POWER CONTROL/RESET REGISTER

Addr	Name/Desc.	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x02	**PWR_CTRL_RST_REG Power Control/Reset Register**	POR_RESET	**RESV**	FIFO_RESET	XL_RESET	HOLD_DISABLE	OTP_PWR_EN	FIFO_PWR_EN	XL_PWR_EN	0x00	R/W

Bit	Name	Description
0	XL_PWR_EN	0: XL VDD power is disabled (default). 1: XL VDD power is enabled. This bit enables power to the XL/WAKE power domain. **If the PWR_MODE[2:0] bits in register 0x05 are configured as LP2 or LP3 for duty-cycle sampling of the XL power domain, this bit should be '0' so that the XL state machine can automatically manage the power. Use the WAKE operational mode in register 0x04 to enable XL operation.** **Also see register 0x56 bit 1, DIS_XL_AUTO_RESET (section 6.1.56).**
1	FIFO_PWR_EN	0: FIFO VDD power is disabled (default). 1: FIFO VDD power is enabled. This bit enables power to the FIFO control logic and storage.
2	OTP_PWR_EN	0: OTP VDD power is disabled (default). 1: OTP VDD power is enabled. This bit enables power to the OTP core.
3	HOLD_DISABLE	0: Holding/isolation cells are enabled (default). 1: Holding/isolation cells are disabled. When a power domain is disabled, any output signals from that domain are held at known levels (usually logic '0'). T**his bit must be set to '1' to allow signals from the XL or FIFO power domains to pass into the SYS power domain**. Note this bit will not release the holding cells if power is not applied to the XL or FIFO domains.
4	XL_RESET	0: XL reset is not asserted (default). 1: XL reset is asserted. This active high reset must be set and cleared by software.
5	FIFO_RESET	0: FIFO reset is not asserted (default). 1: FIFO reset is asserted. This active high reset must be set and cleared by software.
6	RESV	Reserved.
7	POR_RESET	0: POR reset is not asserted (default). 1: POR reset is asserted. This active high reset will execute a POR/boot reset.

Table 6-1: Register Pg0 0x02 bit assignments

6.1.4 0X03 – DEVICE STATUS REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x03	**DEV_STATUS Device Status 3 Register**	BOOT_ STATUS	**RESV**	FIFO_ HOLD_ STATUS	XL_HOLD_ STATUS	**RESV**	OTP_PWR_ GOOD	FIFO_PWR _GOOD	XL_PWR_ GOOD	0x30	RO

Bit	Name	Description
0	XL_PWR_GOOD	0: XL power is disabled (default). 1: XL power status is good.
1	FIFO_PWR_GOOD	0: FIFO power is disabled (default). 1: FIFO power status is good.
2	OTP_PWR_GOOD	0: OTP power is disabled (default). 1: OTP power status is good.
3	**RESV**	Reserved
4	XL_HOLD_ STATUS	0: XL holding/isolation cells are not in hold. 1: XL holding/isolation cells are in hold (default). Enabling XL power in register 0x02 bit 0 and setting 0x02 bit 3 will disable the holding cells and clear this status bit.
5	FIFO_HOLD_STATUS	0: FIFO holding/isolation cells are not in hold. 1: FIFO holding/isolation cells are in hold (default). Enabling FIFO power in register 0x23 bit 2 and setting 0x23 bit 3 will disable the holding cells and clear this status bit.
6	**RESV**	Reserved
7	BOOT_STATUS	0: Boot is in completed (default). 1: Boot is in progress.

Table 6-2: Register 0x03 assignments

6.1.5 0X04 – CONTROL REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x04	CTRL_REG_1 Control Register 1	TEMP_ SENSE_EN	Z_PD	Y_PD	X_PD	SLOW_CLK[1:0]		STATE[1:0]		0x00	R/W

Bit	Name	Description
1:0	STATE[1:0]	00: SLEEP Mode (default) 01: WAKE Mode 10: SELF TEST Mode 11: STANDBY Mode The STATE bits set the operation mode for Atria.
3:2	SLOW_CLK[1:0]	00: Slow clock is SYS_OSC / 32 (default) 01: Slow clock is SYS_OSC / 64 10: Slow clock is SYS_OSC / 128 11: Slow clock is SYS_OSC / 256 This selects the frequency of the 'slow clock' when dynamic clock switching is enabled. Register 0x05 bit 7 must be set to '1' for the dynamic clock switching feature to be enabled.
4	X_PD	0: X-channel is enabled in WAKE mode. (default) 1: X-channel is disabled.
5	Y_PD	0: Y-channel is enabled in WAKE mode. (default) 1: Y-channel is disabled.
6	Z_PD	0: Z-channel is enabled in WAKE mode. (default) 1: Z-channel is disabled.
7	TEMP_SENSE_EN	0: Temperature sensor is disabled. (default) 1: Temperature sensor is enabled.

SLOW_CLK[1:0]	SYS_OSC = 1.6 MHJz	SYS_OSC = 200 kHz
00	50 kHz	6.25 KHz
01	25 kHz	3.125 kHz
10	12.5 kHz	1.5625 kHz
11	6.25 kHz	0.78125 kHz

Table 6-3: Register 0x04 assignments

6.1.5.1 SLEEP MODE

SLEEP mode is the default mode following a POR or soft-reset. Note configuring SLEEP mode in register 0x04 does not override the power domain controls in register 0x02.

6.1.5.2 WAKE MODE

WAKE mode is used for continuous or duty-cycled sampling of the XL. If the PWR_MODE[2:0] bits are configured in register 0x05, the XL power domain may be power-cycled automatically between samples.

MEMSIC

6.1.5.3 SELF-TEST MODE

The self -test mode uses the 'tilt and release' feature of the MEMS to capture data and write it to the FIFO. The self-test data captured only comes from the sinc filter output. The following table shows basic usage of the self-test mode.

Step	Description	Operation
0	Enable power domains FIFO on, XL on, HOLD_DISABLE	W: 0x02 <= 0x0B
1	Enable FIFO	W: 0x13 <= 0x60
2	Set oscillator frequency (recommend 1.6 MHz).	W: 0x05 <= 0x00
3	Go to STANDBY mode	W: 0x04 <= 0x03
4	Set OSR (OSR 64).	W: 0x06 <= 0x10
5	Set SINC filter level (SINC2 in this example).	W: 0x07 <= 0x00
6	Set the decimation count to SINC order + 1.	W: 0x22 <= 0x00
7	Set TILT hold time. This is approximately 10ms.	W: 0x92 <= 0x20
8	Set the self-test sample ignore count (defaults to 20 decimal).	W: 0x94 <= 0x14
9	Select the channel for self-test, X-axis in this example.	W: 0x9C <= 0x01
10	Set the self-test detection threshold.	W: 0xAB <= LSB W: 0xAC <= MSB
11	Set the self-test detection interrupt. Disable and clear all interrupts, the enable self-test interrupt.	W: 0x24 <= 0x00 W: 0x10 <= 0xFF W: 0x11 <= 0xFF W: 0x24 <= 0x01
12	Execute self-test	W: 0x04 <= 0x02
13	Poll register 0x18 until FIFO full transitions to '1' (bit 1)	R: 0x18 <= 0xXX … R: 0x18 <= 0x03
14	Another way to detect the self-test interrupt to check that FIFO is full and self-test is terminated.	R: 0x10 <= 0x01
15	Read self-test detection results	R: 0x12 <= bit[0] 0: fail 1: Pass
16	Read contents of FIFO, 96 16-bit samples of X-data.	for loop = 1 to 32: burst_read(0x19,0x1A,0x1B,0x1C,0x1D,0x1E)

17	Return to STANDBY state to reset XL state machine.	W: 0x04 <= 0x03

Table 6-4: Self-test basic operation

6.1.5.4 STANDBY MODE

STANDBY mode is defined as no active XL sampling, but the system oscillator/clock is running. This is useful for trimming analog reference currents/voltage and the system oscillator. Note configuring STANDBY mode in register 0x04 does not override the power domain controls in register 0x02.

MEMSIC

6.1.6 0X05 – CONTROL REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x05	**CTRL_REG_2 Control Register 2**	DUTY_CYC_CLK_EN	CLK_SEL[2:0]			LOW_PWR_EN	PWR_MODE[2:0]			0x00	R/W

Bit	Name	Description			
2:0	PWR_MODE[2:0]	**PWR_MODE[2:0]**	**Sampling Mode**	**Analog Power Management**	**Digital Power Management**
		000 (Normal)	Duty Cycled	Disabled	Disabled
		001 (LP1)	Duty Cycled	Enabled	Disabled
		010 (LP2)	Duty Cycled	Disabled	Enabled
		011 (LP3)	Duty Cycled	Enabled	Enabled
		100 (High Power)	Continuous	None	None
		PWR_MODE[2:0] selects the sampling mode and power management mode. If motion detection features are to be used select Normal, LP1, or High-Power modes. **If the PWR_MODE[2:0] bits are configured for duty-cycle sampling of the XL power domain, register 0x02 bit 0 should be '0' so that the XL state machine can automatically manage the power.** **Also see register 0x56 bit 1, DIS_XL_AUTO_RESET (section 6.1.56).**			
3	LOW_ANA_PWR_EN	0: Additional analog low power features disabled (default). (See reg 0x88 bits 4:3) 1: Additional analog low power features enabled. When this bit is enabled, additional analog features can be added to the analog power management in PWR_MODEs 0-3 above. Normally, only the ADC/SDMs are disabled between samples. Register 0x88 bit 3 allows the ALDO (analog LDO) to be disabled, and 0x88 bit 4 allows the IBIAS generator to be disabled. Note there are performance tradeoffs for more aggressive power management.			
6:4	CLK_SEL[2:0]	Select the main clock frequency. The main clock divider generates the corresponding frequency as shown below. Note there are two SYS_OSC frequencies from the analog. This clock frequency is used for active sampling. If 0x05 bit 7 (clock duty cycling) is enabled, the clock frequency used between sampling is determined by register 0x04 bits 3:2.			
		CLK_SEL[2:0]	**SYS_OSC = 1.6 MHz (Reg 0x20 bit 6 = 0)**	**SYS_OSC = 200 kHz (Reg 0x20 bit 6 = 1)**	**Notes**
		000	1.6 MHz	200 kHz	
		001	800 kHz	100 kHz	
		010	400 kJz	50 kHz	
		011	200 KHz	25 kHz	

		100	72.727 kHz	9.091 kHz	
		101	32 kHz	4 kHz	
		110	32 kHz	4 kHz	
		111	16 kHz	2 kHz	
7	DUTY_CYC_CLK_EN	0: Duty cycle clock feature is disabled (default). 1: Duty cycle clock feature is enabled. This feature allows the system clock frequency to be slowed between active samples. This option lowers overall device power and is required to reach the lowest power modes. This bit must be selected before entering LP1/2/3 low power modes.			

Table 6-5: Register 0x05 assignments

MEMSIC

6.1.6.1 POWER MODES VS SINC/SDM MODES

0x05 [2:0] PWR_MODE	Sampling Mode	Analog Power Management	Digital Power Management
000 (Normal)	Duty Cycled	Disabled	Disabled
001 (LP1)	Duty Cycled	Enabled	Disabled
010 (LP2)	Duty Cycled	Disabled	Enabled
011 (LP3)	Duty Cycled	Enabled	Enabled
100 (LN, low noise)	Continuous	None	None

Table 6-6: Power Modes

No.	Pwr Mode	Sinc/SDM Mode	OSR XY	WAF Z	OSR Z	WAF Z	XY vs Z	IDR	Comment
1	Ultra low power mode	LPA	osr1	1/bypass	osr1	1/bypass	Non-Overlap	x=y=z	IDR=ODR
2	low power mode WAF	LPA	osr1	waf_1	osr1	waf_1		x=y=z	IDR=ODR
3	double z low power mode	LPB	osr1	1/bypass	osr1	2		x=y=z	IDR=ODR
4	double z low powr mode WAF	LPB	osr1	waf1	osr1	waf1*2		x=y=z	IDR=ODR
5	double z low noise mode WAF	LPB	osr1	waf1 (maximum waf)	osr1	waf1*2		x=y=z	IDR=ODR
6	low power mode (Z-higher WAF)	LPC	osr1	1/bypass	osr1	4	Overlap	x=y=z	IDR=ODR
7A	lower noise mode (Z higher WAF)	LPC	osr1	waf1	osr1	waf2 = waf1*2+2		x=y=z	IDR=ODR
7B	Low noise mode (Z higher WAF)	LPC	osr1	Waf1 (maximum waf)	Osr1	waf2 = waf1*2+2		X=y=z	IDR=ODR
8	lower power mode (higher OSR z)	LPD	osr1	1/bypass	osr1*2	1/bypass		x=y=z	IDR=ODR
9A	lowest power mode	LN	osr1	waf1	osr2	waf2		y=x y!=z	yIDR=ODR zIDR>=ODR

Table 6-7: Power modes vs SINC/SDM sampling modes

6.1.7 0X06 – CONTROL REGISTER 3

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x06	CTRL_REG_3 Control Register 3	RESV	OSR[2:0]			XL_G_RANGE[3:0]				0x10	R/W

Bit	Name	Description		
3:0	XL_G_RANGE[3:0]	Select the G-range scaling used for XL X/Y/Z data. Note that the 32g or 48g full range setting will impact TCO and TCS temperature coefficient settings.		
		XL_G_RANGE[3:0]	**G-Range**	**Notes**
		0x0	+/-2g	Based on 48g total range
		0x1	+/-4g	Based on 48g total range
		0x2	+/-8g	Based on 48g total range
		0x3	+/-16g	Based on 48g total range
		0x4	+/-12g	Based on 48g total range
		0x5	+/- 24g	Based on 48g total range
		0x6, 0x7	Not used	N/A
		0x8	+/-2g	Based on 32g total range
		0x9	+/-4g	Based on 32g total range
		0xA	+/-8g	Based on 32g total range
		0xB	+/-16g	Based on 32g total range
		0xC,0xD,0xE,0xF	Not used.	N/A
6:4	OSR[2:0]	Select the oversampling ratio used by the main sinc filters. This becomes the decimation rate output of the main sinc filters.		
		OSR[2:0]	**Selected OSR**	**Notes**
		000	32	Sinc filter output rate is Fs/32.
		001	64	Sinc filter output rate is Fs/64.
		010	125	Sinc filter output rate is Fs/128.
		011	256	Sinc filter output rate is Fs/256.

		100	512	Sinc filter output rate is Fs/512.
7	RESV	Reserved.		

Table 6-8: Register 0x06 assignments

MEMSIC

6.1.8 0X07 – CONTROL REGISTER 4

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x07	**CTRL_REG_4 Control Register 4**	XL_AVG_ FILTER_XY_ EN	**RESV**	SINC_ODR[1:0]		LPF_PASS_ THRU_Z	LPF_RESET	LPF_PASS _THRU_XY	LPF_EN	0x03	R/W

Bit	Name	Description
0	LPF_EN	0: LPF filter is disabled. 1: LPF filter is enabled (default) The 2nd order Butterworth low pass filter is enabled by default. Unique cutoff frequencies Fc require that filter coefficient registers to the programmed. X and Y axis coefficients: registers 0x4E to 0x57 Z axis coefficients: registers 0xAD to 0xB4
1	LPF_PASS_THRU_XY	0: LPF XY filter is set to normal mode (requires coefficients to be programmed) 1: LPF XY filter is set to pass thru, coefficients are set to '1'. The 2nd order Butterworth low pass filter 'pass-thru' mode allows data to run through the filter with coefficients set to '1'.
2	LPF_RESET	0: LPF is not reset (default). 1: LPF is reset. The bit resets the registers in the LPF. This reset is an active high level and must be set/cleared by SW.
3	LPF_PASS_THRU_Z	0: LPF Z filter is set to normal mode (requires coefficients to be programmed) 1: LPF Z filter is set to pass thru, coefficients are set to '1'. The 2nd order Butterworth low pass filter 'pass-thru' mode allows data to run through the filter with coefficients set to '1'.
5:4	SINC_ODR	00: SINC filter order is 2. (default) 01: SINC filter order is 3.
6	**RESV**	Reserved.
7	XL_XY_AVG_FILTER_EN	0: XL XY averaging filter is disabled (default). 1: XL XY averaging filter is enabled.

Table 6-9: Register 0x07 assignments

6.1.9 0X08 TO 0X0D – XL OUTPUT REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
08	**XL_XOUT_LSB**	XL_XOUT[7:0]								0x00	RO
09	**XL _XOUT_MSB**	XL_XOUT[15:8]								0x00	RO
0A	**XL_YOUT_LSB**	XL_XOUT[7:0]								0x00	RO
0B	**XL _YOUT_MSB**	XL_YOUT[15:8]								0x00	RO
0C	**XL _ZOUT_LSB**	XL_ZOUT[7:0]								0x00	RO
0D	**XL _ZOUT_MSB**	XL_ZOUT[15:8]								0x00	RO

Registers 0x08 to 0x13 contain the signed output values read from the X, Y, and Z accelerometer channels. The values are represented as a signed, 2's compliment 16-bit number. Values will range from 0x8000 (full scale negative) to 0x7FFF (full scale positive). The actual output range will be affected by the selected g-range and the analog gain of the SDM. If the FIFO is enabled, FIFO output data is read from registers 0x19 to 0x1E.

MEMSIC

6.1.10 0X0E, 0X0F – TEMPERATURE OUTPUT DATA

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x0E	TEMP_DATA_LSB	TEMP_DATA[7:0]								0xE8	RO
0x0F	TEMP_DATA_MSB	RESV					TEMP_DATA [10:8]			0x03	RO

This register reports the raw temperature sensor output. This value is not corrected or modified for any factory trim values. For the corrected temperature with the factory trim value, use registers 0xA9, 0xAA.

MEMSIC

6.1.11 0X10, 0X11 – INTERRUPT STATUS AND CLEAR REGISTERS 1/2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x10	**INT_REG_1 Interrupt Status Register 1**	FLIP_ INTR	TF_ INTR	FIFO_ INTR	NO_MOTION_ INTR	SHAKE_ INTR	ANYM_ INTR	XL_SAMPLE_ INTR	SLFTST_ INTR	0x00	R
0x10	**INT_CLR_REG_1 Interrupt Clear Register 1**	FLIP_ INTR_CLR	TF_ INTR_CLR	FIFO_ INTR_CLR	NO_MOTION_ INTR_CLR	SHAKE_ INTR_CLR	ANYM_ INTR_CLR	XL_SAMPLE_ INTR_CLR	SLFTST_ INTR_CLR	0x00	W1C
0x11	**INT_CLR_REG_2 Interrupt Status Register 2**	**RESV**	INT1_ MOTION-LESS_INTR	**RESV**	FREEFALL_ INTR	SIXD_INTR	TTAP_INTR	DTAP_INTR	TAP_INTR	0x00	R
0x11	**INT_CLR_REG_2 Interrupt Clear Register 2**	**RESV**	INT1_ MOTION-LESS_CLR	**RESV**	FREEFALL_ INTR_CLR	SIXD_INTR_ CLR	TTAP_INTR_ CLR	DTAP_INTR_ CLR	TAP_INTR_ CLR	0x00	W1C

Registers 0x10 and 0x11 have separate read and write paths. Hardware sets interrupts in this register. To clear an interrupt, write a bitmask with the bit to clear set to '1' to register 0x10 or 0x11 (write 1 to clear, W1C). **There is no need to write a '0' to clear the '1', it is auto-clearing**.

Also note that the corresponding interrupt must be enabled in registers 0x24 or 0x25. Note that FIFO interrupts are serviced in register 0x18.

Bit	Name	Description
0	SLFTST_INTR_CLR	0: Self-test interrupt has not been detected. 1: Self-test interrupt has been detected. Write '1' to this bit to clear.
1	XL_SAMPLE_INTR	0: No new XL sample data has arrived since last read. 1: New XL sample data has arrived and has been written to the output registers. Write '1' to this bit to clear.
2	ANYM_INTR	0: Any motion event/interrupt is not detected. 1: Any motion event/interrupt detected. Write '1' to this bit to clear.
3	SHAKE_INTR	0: SHAKE event/interrupt is not detected. 1: SHAKE event/interrupt detected.

4	NOMO_INTR	0: NoMotion event/interrupt not detected 1: NoMotion event/interrupt detected. Write '1' to this bit to clear.
5	FIFO_INTR	0: No FIFO interrupt has been detected. 1: FIFO interrupt has been detected. Write '1' to this bit to clear. Register 0x18 bits 2:0 report which FIFO interrupt condition was triggered (FIFO_EMPTY, FIFO_FULL, FIFO_THRESH).
6	TILT_INTR	0: TILT event/interrupt is not detected. 1: TILT event/interrupt detected. Write '1' to this bit to clear.
7	FLIP_INTR	0: FLIP event/interrupt is not detected. 1: FLIP event/interrupt detected. Write '1' to this bit to clear.

Table 6-10: Register 0x10 bit assignments

Bit	Name	Description
0	TAP_INTR	0: Tap event/interrupt has not been detected. 1: Tap event/ interrupt has been detected. Write '1' to this bit to clear.
1	DTAP_INTR	0: Double Tap event/interrupt has not been detected. 1: Double Tap event/ interrupt has been detected. Write '1' to this bit to clear.
2	TTAP_INTR	0: Triple Tap event/interrupt has not been detected. 1: Triple Tap event/interrupt has been detected. Write '1' to this bit to clear.
3	SIXD_INTR	0: Change in 6D origination threshold/interrupt not detected. 1: Change in 6D origination threshold/interrupt detected. Write '1' to this bit to clear.
4	FREEFALL_INTR	0: Freefall event/interrupt has not been detected. 1: Freefall event/interrupt has been detected Write '1' to this bit to clear.
5	**RESV**	Reserved.
6	MOTIONLESS_INTR	0: MOTIONLESS interrupt has not been detected. 1: MOTIONLESS has been detected Write '1' to this bit to clear.
7	**RESV**	Reserved.

Table 6-11: Register 0x11 bit assignments

6.1.12 0X12 – SENSOR AND MOTION STATUS REGISTER (STATUS REGISTER)

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
Pg0 0x12	Status Register 1	FLIP_FLAG	TF_FLAG	FIFO_FLAG	NO_MO_STAT	SHAKE_FLAG	ANYM_FLAG	NEW_DATA_XL_STAT	SLFTST_STATUS	0x30	RO

Note that Motion register default values such as NO_MO_STAT is set under XL power domain. It needs to enable XL_PWR_EN(Refer to register 0x02 bit0) and to disable hold/isolation cells(Refer to register 0x02 bit3) to get motion register default values.

Bit	Name	Description
0	SLFTST_STATUS	Shows the results of the XL self-test sequence. 0: Self-test not run or fail (default). 1: Self-test passed. This is the self-test pass/fail indicator. Refer to register 0x97 bit 7 for the self-test 'done' indicator.
1	NEW_DATA_XL_STAT	0: No new sample data has arrived since last read. (default) 1: New sample data has arrived and has been written output registers.
2	ANYM_STAT	0: Any motion condition is not detected. 1: Any motion condition detected.
3	SHAKE_STAT	0: SHAKE condition is not detected. 1: SHAKE condition detected.
4	NO_MO_STAT	0: No Motion condition is not detected. 1: No Motion condition is detected.
5	FIFO_FLAG	0: No FIFO flags set. 1: FIFO flag is set (FIFO full, FIFO empty, FIFO threshold).
6	TILT_STAT	0: TILT condition is not detected. 1: TILT condition detected.
7	FLIP_STAT	0: FLIP condition is not detected. 1: FLIP condition detected.

Table 6-12: register 0x12 bit assignments

6.1.13 0X13 – FIFO CONTROL REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x13	**FIFO_CTRL_1 FIFO Control Register 1**	**RESV**	FIFO_READ_EN	FIFO_ ENABLE	FIFO_STREAM _MODE	**RESV**	FIFO_EMPTY_INTR_EN	FIFO_FULL_ INTR_EN	FIFO_ THRESH_ INTR_EN	0x00	R/W

Bit	Name	Description
0	FIFO_THRESH_INTR_EN	0: FIFO threshold feature and interrupt is not enabled. (default) 1: FIFO threshold feature and interrupt is enabled.
1	FIFO_FULL_INTR_EN	0: FIFO full feature and interrupt is not enabled. (default) 1: FIFO full feature and interrupt is enabled.
2	FIFO_EMPTY_INTR_EN	0: FIFO empty feature and interrupt is not enabled. (default) 1: FIFO empty feature and interrupt is enabled.
3	**RESV**	Reserved.
4	FIFO_STREAM_MODE	0: FIFO stream mode is disabled (default). 1: FIFO stream mode is enabled. FIFO stream mode allows the FIFO to capture any new data on the write port, while removing the oldest previously captured sample.
5	FIFO_ENABLE	0: FIFO is disabled (default). 1: FIFO is enabled. This is the main FIFO enable. Note that the FIFO DVDD domain must be enabled/powered also.
6	FIFO_READ_EN	0: FIFO is not in read mode (default). 1: FIFO is in read mode. Set this bit to '1' to enable the FIFO_DOUT port in registers 0x19 to 0x1E.
7	**RESV**	Reserved.

Table 6-13: register 0x13 bit assignments

6.1.14 0X14 – FIFO CONTROL REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x14	FIFO_CTRL_2 FIFO Control Register 2	RESV	RESV	RESV	FIFO_THRESH[4:0]					0x00	R/W

Bit	Name	Description
4:0	FIFO_THRESH[4:0]	The FIFO threshold or 'watermark' sets the number of FIFO samples at which the FIFO threshold flag/interrupt is set.
7:5	**RESV**	Reserved.

Table 6-14: register 0x14 bit assignments

MEMSIC

6.1.15 0X15 – FIFO CONTROL REGISTER 3

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x15	**FIFO_CTRL_3 FIFO Control Register 3**	**RESV**	**RESV**	FIFO_ BURST_ READ	FIFO_BURST_LEN[4:0]					0x00	R/W

Bit	Name	Description
4:0	FIFO_BURST_LEN [4:0]	The FIFO burst length sets the number of samples to read in a single serial (SPI, I2C, I3C) read transaction.
5	FIFO_BURST_READ	0: FIFO burst read mode is not enabled (default). 1: FIFO burst read mode is enabled.
7:6	RESV	Reserved.

Table 6-15: register 0x15 bit assignments

MEMSIC

6.1.16 0X16 – FIFO STATUS REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x16	**FIFO_STAT_2 FIFO Status Register 1**	FIFO_WPTR[5:4]		FIFO_RPTR[5:0]						0x00	RO

Bit	Name	Description
5:0	FIFO_RPTR[5:0]	FIFO Read pointer – this reports the current value of the FIFO read pointer. This value may be indeterminant during FIFO stream mode while new samples are being captured to the FIFO.
7:6	FIFO_WPTR[5:4]	FIFO Write pointer – these bits form bits 5:4 of the 6-bit FIFO_WPTR[5:0] value.

Table 6-16: register 0x16 bit assignments

MEMSIC

6.1.17 0X17 – FIFO STATUS REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x17	**FIFO_STAT_2 FIFO Status Register 2**	WPTR_ STREAM	RPTR_ STREAM	FIFO_SAMPLE_CNT[5:0]						0x00	RO

Bit	Name	Description
5:0	FIFO_SAMPLE_CNT[5:0]	This value reports the number of samples currently stored in the FIFO. Note that this value may dynamically change and samples are written or read to/from the FIFO.
6	RPTR_STREAM	0: FIFO read pointer is operating normally. 1: FIFO read pointer is operating in stream mode or has not been enabled (default). This bit operates only if FIFO_STREAM mode has been enabled - disregard the FIFO read pointer value in register 0x16 bits 5:0. If the device is reset or the FIFO has not been initialized, this bit will also be set even through FIFO stream mode is not active.
7	WPTR_STREAM	0: FIFO write pointer is operating normally. 1: FIFO write pointer is operating in stream mode or has not been enabled (default). This bit operates only if FIFO_STREAM mode has been enabled - disregard the FIFO write pointer value in registers 0x16 and 0x18. If the device is reset or the FIFO has not been initialized, this bit will also be set even through FIFO stream mode is not active.

Table 6-17: register 0x17 bit assignments

MEMSIC

6.1.18 0X18 – FIFO STATUS REGISTER 3

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x18	FIFO_STAT_3 FIFO Status Register 3	FIFO_WPTR[3:0]				FIFO_ OVERRIUN	FIFO_ EMPTY	FIFO_FULL	FIFO_ THRESH	0x04	RO

Bit	Name	Description
0	FIFO_THRESH	0: FIFO threshold has not been reached (default). 1: FIFO threshold has been reached. Note this flag only operates if the FIFO_THRESH_INT_EN bit has been set in register 0x13 bit 0.
1	FIFO_FULL	0: FIFO is not full (default). 1: FIFO is full. Note this flag only operates if the FIFO_FULL_INT_EN bit has been set in register 0x13 bit 1.
2	FIFO_EMPTY	0: FIFO is not empty. 1: FIFO is empty (default).
3	FIFO_OVERRUN	0: FIFO is not overrun (default) 1: FIFO is overrun.
7:4	FIFO_WPTR[3:0]	FIFO Write pointer – these bits form bits 3:0 of the 6-bit FIFO_WPTR[5:0] value.

Table 6-18: register 0x18 bit assignments

MEMSIC

6.1.19 0X19 TO 0X1E – FIFO_DOUT REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x19	FIFO_XOUT_LSB	FIFO_XOUT[7:0]								0x00	RO
0x 1A	FIFO_XOUT_MSB	FIFO_XOUT[15:8]								0x00	RO
0x 1B	FIFO_YOUT_LSB	FIFO_YOUT[7:0]								0x00	RO
0x 1C	FIFO_YOUT_MSB	FIFO_YOUT[15:8]								0x00	RO
0x1D	FIFO_ZOUT_LSB	FIFO_ZOUT[7:0]								0x00	RO
0x 1E	FIFO_ZOUT_MSB	FIFO_ZOUT[15:8]								0x00	RO

Reg/Bit	Name	Description
0x19 7:0	FIFO_DOUT[7:0] FIFO_XOUT[7:0]	Normal Mode: FIFO_DOUT[47:0] – 6 bytes representing data read from the FIFO, each channel X, Y, Z uses 2-bytes. Self-Test Mode FIFO_DOUT[47:0] - – 6 bytes representing data read from the FIFO, one channel (X, Y or Z) uses 2-bytes to store 3-samples from the same axis. Note that live-data mode or non-FIFO captured data is reported in registers 0x08 to 0x0D.
0x1A 7:0	FIFO_DOUT[15:8] FIFO_XOUT[15:8]	
0x1B 7:0	FIFO_DOUT[23:16] FIFO_YOUT[7:0]	
0x1C 7:0	FIFO_DOUT[31:24] FIFO_YOUT[15:8]	
0x1D 7:0	FIFO_DOUT[39:32] FIFO_ZOUT[7:0]	
0x1E 7:0]	FIFO_DOUT[47:40] FIFO_ZOUT[15:8]	

Table 6-19: registers 0x19-0x1E bit assignments

6.1.20 0X1F - ODR DIVIDE REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x1F	**ODR_DIV ODR Divide Register**	ODR_DIV[7:0]								0x00	RW

Bit	Name	Description
7:0	ODR_DIV[7:0]	8-bit divide value used to select the XL output data rate for sampling. The ODR_PRE_CLK frequency, selected by register 0x20 [1:0], is divided by the 8-bit value in register 0x1F. See section 6.1.21. **ODR = ODR_PRE_CLK_SEL / ODR_DIV**

Table 6-20: register 0x1F bit assignments

MEMSIC

6.1.21 0X20 – ODR PRESCALE REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x20	**ODR_PRESCALE ODR Prescale Register**	SYS_OSC_EN	SYS_OSC_LOW_EN	**RESV**	OFFSET_SEL	UPD_MODE_SEL	**RESV**	ODR_CLK_SEL[1:0]		0x00	R/W

Bit	Name	Description
1:0	ODR_CLK_SEL[1:0]	Select the ODR prescale clock used to generate an ODR. Register 0x1F ODR_DIV[7:0] determines the divide by value of the ODR_PRESCALE clock. For example: • 0x20[1:0] = 10 or 6.25 kHz, Select ODR_CLK_SEL • 0x1F[7:0] = 'd62 (0x3E), Program ODR_DIV value • XL ODR = 6.25 kHz / 62 = ~100.8 Hz, Resulting ODR rate

ODR_PRE_CLK[1:0]	SYS_OSC = 1.6 MHz	SYS_OSC = 200 kHz
00 (div by 1)	1.6 MHz	200 kHz
01 (div by 32)	50 kHz	6.25 kHz
10 (div by 256)	6.250 kHz	781.25 Hz
11 (div by 16384)	97.6 Hz	12.2 Hz

2	**RESV**	Reserved
3	UPD_MODE_SEL	0: ODR clock determines when the XL output registers are updated (default). 1: Output registers are updated by XL pipeline rate (option for continuous mode).
4	OFFSET_SEL	0: XL offset selection is registers 0x58 to 0x5D (default). 1: XL offset selection is registers 0x5E to 0x61, 0x6C and 0x79.
5	**RESV**	Reserved
6	SYS_OSC_LOW	0: System oscillator frequency is ~1.6 MHz (default). 1: System oscillator frequency is ~200 kHz. When the system oscillator frequency is 1.6 MHz, the OTP backed trim value is at register 0x81. When the system oscillator frequency is 200 kHz MHz, the trim value is at register 0x82. During boot, the system oscillator trim is automatically set to 0x50.
7	SYS_OSC_EN	0: System oscillator is disabled or under hardware control (register 0x04 bits 1:0) (default). 1: System oscillator is manually enabled by this bit. The system oscillator is automatically enabled during STANDBY and WAKE modes, or if the device reset is active.

Table 6-21: register 0x20 bit assignments

6.1.22 0X21 – TEMP CONTROL

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x21	TEMP_CTRL Temp Control Register	TEMP_CAL_EN	TEMP_SENSE_RESET	**RESV**	**RESV**	TCO_TCS_DEBUG[1:0]		TCS_BYPASS	TCO_BYPASS	0x00	R/W

Bit	Name	Description
0	TCO_BYPASS	0: Temperature controlled (compensation) offset adjustment is not bypassed (default). 1: Temperature controlled (compensation) offset is bypassed.
1	TCS_BYPASS	0: Temperature controlled (compensation) sensitivity adjustment is not bypassed (default). 1: Temperature controlled (compensation) sensitivity is bypassed.
3:2	TCO_TCS_DEBUG [1:0]	**TCO_TCS_DEBUG [1:0] (Select debug output)** / **TCO Debug (0xA6[7:0], 0xA8[4:0])** / **TCS Debug (0xA7[7:0], 0xA8 bit 7)** 00 / Disabled / Disabled 01 / TCO X-axis Parallel Data TCO_X_PDATA[12:0] / TCS X-axis Parallel Data TCS_X_PDATA[8:0] 10 / TCO Y-axis Parallel Data TCO_Y_PDATA[12:0] / TCO Y-axis Parallel Data TCS_Y_PDATA[8:0] 11 / TCO Z-axis Parallel Data TCO_Z_PDATA[12:0] / TCO Z-axis Parallel Data TCS_Z_PDATA[8:0]
4	**RESV**	Reserved.
5	**RESV**	Reserved.
6	TEMP_SENSE_RESET	0: The analog temperature sensor is not reset (default). 1: The analog temperature sensor is reset (level).
7	TEMP_CAL_EN	0: Temperature sensor calibration is not enabled (default). 1: Temperature sensor calibration is enabled.

Table 6-22: register 0x21 bit assignments

6.1.23 0X22 – XL XY DECIMATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x22	XL_XY_DEC_REG XL Decimation Register for XY	XL_XY_DEC_COUNT[7:0]								0x04	R/W

Bit	Name	Description
7:0	XL_XY_DEC_COUNT[7:0]	Set the decimation count for the XL XY channels; does not apply to Z. The XL XY averaging filter must be enabled for the decimation count to apply (register 0x07 bit 7 = '1'), otherwise the count is set to 1. 0x00: Decimation count is 256 (default). 0x01-0xFF, decimation count is 1 to 255. Also see register 0x90, the Z-axis decimation count.

Table 6-23: register 0x22 bit assignments

MEMSIC

6.1.24 0X23 – INTERRUPT CONTROL REGISTER 0

This register selects which interrupt(s) are connected to the external INT1 and INT2 pads.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x23	INT_CTRL_0 Interrupt Control Register 0	INT2_SEL[3:0]				INT1_SEL[3:0]				0x00	R/W

Bit	Name	Description
3:0	INT1_SEL[3:0]	Select which interrupt drives the INT1 pad. 0: Default (XL sample/Motion or **ALL** interrupts), set register 0x26 bit 4 to combine all interrupts) 1: **Reserved** 2: XL interrupt on sample 3: Shake 4: AnyMotion/NoMotion 5: Flip 6: Tilt 7: **Reserved** 8: Tap 9: Double Tap A: Triple Tap B: Freefall C: Six 6D Orientation D: FIFO Interrupt E: Self-Test State Flag F: **Reserved**
7:4	INT2_SEL[3:0]	Select which interrupt drives the INT2 pad. 0: Default (FIFO or **ALL** interrupts), set register 0x26 bit 4 to combine all interrupts) 1: **Reserved** 2: XL interrupt on sample 3: Shake 4: AnyMotion/NoMotion 5: Flip 6: Tilt 7: **Reserved** 8: Tap 9: Double Tap A: Triple Tap B: Freefall C: Six 6D Orientation D: FIFO Interrupt E: Self-Test State Flag F: **Reserved**

Table 6-24: Register 0x23 bit assignments

6.1.25 0X24 – INTERRUPT CONTROL REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x24	Interrupt Control Register 1	FLIP_ INT_EN	TILT_ INT_EN	RESV	RESV	SHAKE_ INT_EN	ANYM_ INT_EN	ACQ_XL_ INT_EN	SELF_TEST_ INTR_EN	0x00	R/W

Note that the corresponding motion feature in registers 0x2E or 0x2F must be enabled for the interrupt to actual transition.

Bit	Name	Description
0	SELF_TEST_INT_EN	0: Self-Test interrupt is disabled (default) 1: Self-Test interrupt is enabled.
1	ACQ_XL_INT_EN	0: XL interrupt is disabled (default) 1: XL interrupt is enabled.
2	ANYM_INT_EN	0: AnyMotion interrupt is disabled (default) 1: AnyMotion interrupt is enabled.
3	SHAKE_INT_EN	0: Shake interrupt is disabled (default) 1: Shake interrupt is enabled.
4	RESV	Reserved.
5	RESV	Reserved.
6	TILT_INT_EN	0: TILT interrupt is disabled (default) 1: TILT interrupt is enabled.
7	FLIP_INT_EN	0: FLIP interrupt is disabled (default) 1: FLIP interrupt is enabled.

Table 6-25: Register 0x24 bit assignments

6.1.26 0X25 – INTERRUPT CONTROL REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x25	Interrupt Control Register 2	RESV	MOTION LESS_INTR_ EN	NOMO_ INTR_EN	FREEFALL_ INTR_EN	SIXD_ INTR_EN	TTAP_ INTR_EN	DTAP_ INTR_EN	TAP_ INTR_EN	0x00	R/W

Note that the corresponding motion feature in registers 0x2E or 0x2F must be enabled for the interrupt to actual transition.

Bit	Name	Description
0	TAP_INTR_EN	0: TAP interrupt is disabled (default) 1: TAP interrupt is enabled.
1	DTAP_INTR_EN	0: DTAP interrupt is disabled (default) 1: DTAP interrupt is enabled.
2	TTAP_INTR_EN	0: TTAP interrupt is disabled (default) 1: TTAP interrupt is enabled.
3	SIXD_INTR_EN	0: SIXD (6D) interrupt is disabled (default) 1: SIXD (6D) interrupt is enabled.
4	FREEFALL INTR_EN	0: FREEFALL interrupt is disabled (default) 1: FREEFALL interrupt is enabled.
5	NOMO_INTR_EN	0: No Motion interrupt is disabled (default). 1: No Motion interrupt is enabled.
6	MOTIONLESS_INTR_EN	0: Motionless interrupt is disabled (default). 1: Motionless interrupt is enabled.
7	**RESV**	Reserved.

Table 6-26: Register 0x25 bit assignments

6.1.27 0X26 – INT PAD CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x26	INT Pad Control Register	RESV	RESV	RESV	COMB_INTR_EN	INT2_PAD _CFG[1:0]		INT1_PAD_CFG[1:0]		0x00	R/W

Bit	Name	Function	Description
1:0	INT1_PAD_CFG[1:0]	INT1 pad configuration control.	00: INT1 pad operates in interrupt request mode as an output (default). 01: INT1 pad operates in external trigger mode as an input. 10: INT1 pad operates in GPIO mode as a general purpose I/O. 11: INT1 pad operates as a test output. **Important**: When INT1 is configured as a test output for digital test mux 1 (DMUX1), it must be configured in active-drive/push-pull mode. Set register 0x27 bits [3:2] to '11' to enable active-drive mode.
3:2	INT2_PAD_CFG[1:0]	INT2 pad configuration control.	00: INT2 pad operates in interrupt request mode as an output (default). 01: Reserved. 10: INT2 pad operates in GPIO mode as a general purpose I/O. 11: INT2 pad operates as a test output. **Important**: When INT2 is configured as a test output for digital test mux 2 (DMUX2), it must be configured in active-drive/push-pull mode. Set register 0x27 bits [7:6] to '11' to enable active-drive mode.
4	COMB_INTR_EN	Combine all interrupts to the selected INT pad.	0: INT1 and INT2 interrupt sources are not combined (default). 1: INT1 and INT2 interrupt sources are combined. By default, interrupts routed to the INT1 pad are the XL interrupt on sample, self-test interrupt and motion interrupts; interrupts routed to the INT2 pad are any of the FIFO interrupts (0x23 [3:0] = '0000' or 0x23 [7:4] = '0000'). When this bit is set to '1' and 0x23 [3:0] = '0000' or 0x23 [7:4] = '0000', all enabled interrupt sources are combined and sent to INT1 or INT2.
7:5	RESV	Reserved	Reserved.

Table 6-27: Register 0x26 bit assignments

6.1.28 0X27 – GPIO CONTROL REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x27	GPIO_CTRL	GPIO Control Register	GPIO2_ INT2_IPP	GPIO2_ INT2_IAH	GPIO2_ OUT_IN_N	GPIO2_ DATA	GPIO1_ INT1_IPP	GPIO1_ INT1_IAH	GPIO1_ OUT_IN_N	GPIO1_ DATA	0x00	R/W

This register is used to select the INT1 pad and INT2 pad polarity and drive mode when the pads are used as interrupt request outputs, or GPIO outputs.

To use the GPIO functionality for the INT1 pad or the INT2 pad, the INT1_PAD_CFG[1:0] or INT2_PAD_CFG[1:0] control bits in register 0x26 must be set to '10'. The options in this register require GPIO mode to be enabled for the corresponding pad.

Bit	Name	Function	Description
0	GPIO1_DATA	GPIO1 input (read) or output path (write)	Read path, configured as an input (bit 1 = 0) 0: INT1 pad input is at 0. 1: INT1 pad input is at 1. Write path, configured as an output (bit 1 = 1) 0: INT1 pad is driven to a logic 0. 1: INT1 pad is driven to a logic 1. In a read cycle, this bit is used to read the state of the INT1 pad. If the pad is configured as an input, then it returns the current level as read from the pad. If the pad is configured as an output, then this bit is the drive level applied to the pad. In a write cycle, this bit is used to set the state of the pad. If the pad is configured as an output, then this bit determines the drive level applied to the pad.
1	GPIO1_OUT_IN_N	Set the direction of INT1 pad (input or output)	0: INT1 pad is configured as an input (default). 1: INT1 pad is configured as an output.
2	GPIO1_INT1_IAH	Set polarity of INT1 output.	0: The INT1 pad is active low. 1: The INT1 pad is active high. This bit sets the polarity level of the INT1 pad. This bit is used in interrupt mode to set the level of the interrupt request, or in GPIO mode to set the level of the GPIO output drive.
3	GPIO1_INT1_IPP	Select open drain or push/pull mode for INT1.	0: The INT1 pad operates in open-drain mode as an output. 1: The INT1 pad operates in push-pull mode as an output. This bit sets the drive mode of the INT1 pad as an interrupt request output, or a GPIO output.
4	GPIO2_DATA	INT2 input (read) or output path (write)	Read path, configured as an input (bit 1 = 0) 0: INT2 pad input is at 0. 1: INT2 pad input is at 1.

			Write path, configured as an output (bit 1 = 1) 0: INT2 pad is driven to a logic 0. 1: INT2 pad is driven to a logic 1. In a read cycle, this bit is used to read the state of the INT2 pad. If the pad is configured as an input, then it returns the current level as read from the pad. If the pad is configured as an output, then this bit is the drive level applied to the pad. In a write cycle, this bit is used to set the state of the pad. If the pad is configured as an output, then this bit determines the drive level applied to the pad.
5	GPIO2_OUT_IN_N	Set the direction of INT2 pad (input or output)	0: INT2 pad is configured as an input (default). 1: INT2 pad is configured as an output.
6	GPIO2_INT2_IAH	Set polarity of INT2 output.	0: The INT2 pad is active low. 1: The INT2 pad is active high. This bit sets the polarity level of the INT2 pad. This bit is used in interrupt mode to set the level of the interrupt request, or in GPIO mode to set the level of the GPIO output drive.
7	GPIO2_INT2_IPP	Select open drain or push/pull mode for INT2.	0: The INT2 pad operates in open-drain mode as an output. 1: The INT2 pad operates in push-pull mode as an output. This bit sets the drive mode of the INT2 pad as an interrupt request output, or a GPIO output.

Table 6-28: Register 0x27 bit assignments

MEMSIC

6.1.29 0X28 – I3C PARAMETER REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x28	**I3C_PARAM_1 I3C Parameter Register 1**	I3C_RESET	IBI_STATUS_SEL[2]	IBI_STATUS_SEL[2]	IBI_STATUS_SEL[0]	IBI_TRIG	**RESV**	IBI_INTR_REQ_SEL	IBI_EN_INTR	0x00	R/W

Bit	Name	Function	Description
0	IBI_EN_INTR	In-band interrupt enable (I3C only)	0: Interrupts generated from Aries motion, sample or FIFO interrupt sources **do not** generate an in-band interrupt (default). 1: Interrupts generated from Aries motion, sample or FIFO interrupt sources **do** generate an in-band interrupt. This requires the corresponding interrupt enable bits be enabled in registers Pg0 0x20, 0x21 (sample, motion), or Pg0 0x30/0x31 (FIFO).
1	IBI_INTR_REQ_SEL	In-band interrupt request select (I3C only)	0: Source for triggering an IBI is interrupt request 1 (INT1_REQ). 1: Source for triggering an IBI is interrupt request 1 (INT2_REQ).
2	**RESV**	Reserved	Reserved
3	IBI_TRIG	In-band interrupt manual trigger (I3C only)	0: Do not manually trigger an IBI event (default). 1: Trigger a manual IBI event by writing to this bit. This debug bit is intended for generating IBI events via a SW command. This will force Atria to place an IBI request on the I3C bus and wait for master arbitration.
6:4	IBI_STATUS_SEL[2:0]	In-band interrupt status byte select (I3C only)	These three select bits determine the payload of the IBI status byte that is sent to the I3C master. The following selections are available: 0: dev_status_1_i[7:0] – send the contents of register 0x03. 1: intr_status_1_i[7:0] – send the contents of register 0x10. 2: intr_status_2_i[7:0] – send the contents of register 0x11. 3: fifo_status_i[7:0] – send the contents of registers 0x18[2:1], 0x17[5:0]. 4: status_reg_1_i[7:0] – send the contents of register 0x12. 5: Not used . 6: Not used. 7: Not used.
7	I3C_RESET	Local I2C/I3C core reset	0: I3C core is not in reset (default). 1: Apply a reset to the I3C core only (positive edge). This bit applies a local reset to the I2C/I3C core only. This bit will only reset the I3C core and no other parts of Atria. The contents of the registers, pipeline, FIFO, and OTP are not affected. Setting this bit generates a 0->1 transition to the I3C core.

Table 6-29: Register 0x28 bit assignments

6.1.30 0X29 – I3C PARAMETER REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x29	I3C_PARAM_2 I3C Parameter Register 2	I3C_DYNA_ADDR[7]	I3C_DYNA_ADDR[6]	I3C_DYNA_ADDR[5]	I3C_DYNA_ADDR[4]	I3C_DYNA_ADDR[3]	I3C_DYNA_ADDR[2]	I3C_DYNA_ADDR[1]	I3C_DYNA_ADDR[0]	0x00	RO

Bit	Name	Function	Description
7:0	I3C_DYNA_ADDR[7:0]	Dynamically assigned I3C slave address.	This read only register returns the currently assigned I3C slave address. This is **not** the I2C slave address. 0x00: default unassigned address 0xXX: Master assigned I3C slave address (varies).

Table 6-30: Register 0x29 bit assignments

MEMSIC

6.1.31 0X2A – I3C PARAMETER REGISTER 3

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x2A	**I3C Parameter Register 3**	**I3C_ENABLE**	I3C_STATUS_BYTE_SEL[2]	I3C_STATUS_BYTE_SEL[1]	I3C_STATUS_BYTE_SEL[0]	SPI_3WIRE_EN	**RESV**	I3C_PP_MAN_CTRL	I3C_PP_EN	0x80	R/W

Bit	Name	Function	Description
0	I3C_IPP_EN	I3C push-pull control	0: Active drive/push-pull mode for SDA is disabled. (default) 1: Active drive/push-pull mode for SDA is enabled. This bit controls the active drive mode for the SDA pad. This bit is only used when the I3C_PP_MAN_CTRL bit 1 (below) is set to '1'.
1	I3C_PP_MAN_CTRL	Enable manual control of the SDA pad	0: Manual control of SDA drive mode is disabled (default) 1: Manual control of SDA drive mode is enabled. Under typical usage, the I3C core controls the drive mode of the SDA pad.
2	**RESV**	Reserved	Reserved
3	SPI_3WIRE_EN	Enable 3-wire mode for SPI.	0: SPI interface runs in 4-wire mode (default). 1: SPI interface runs in 3-wire mode. In 3-wire mode, SPI read and write data use the SDA pad in bi-directional mode. In 4-wire mode, the SDA pad is used for input data only (MOSI), and the SDO is used for output data (MISO).
6:4	I3C_STATUS_BYTE_SEL[2:0]	Select the payload for the status byte when a GETSTATUS CCC command code is sent by the I3C master.	These three select bits determine the payload of the I3C status byte that is sent to the I3C master on a GETSTATUS command code. The following selections are available: 0: dev_status_1_i[7:0] – send the contents of register 0x03. 1: intr_status_1_i[7:0] – send the contents of register 0x10. 2: intr_status_2_i[7:0] – send the contents of register 0x11. 3: fifo_status_i[7:0] – send the contents of registers 0x18[2:1], 0x17[5:0]. 4: status_reg_1_i[7:0] – send the contents of register 0x12. 5: Not used . 6: Not used. 7: Not used.
7	**I3C_ENABLE**	Enable i3c mode	0: Disable i3c mode. 1: Enable i3c mode. (default)

Table 6-31: Register 0x2A bit assignments

6.1.32 0X2B,0X2C – ANYMOTION MOTION DELTA THRESHOLD

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x2B	MOTION_ DELTA_ THRESH_0	ANYMO_DELTA[7:0]								0x00	R/W
0x2C	MOTION_ DELTA_ THRESH_1	RESV	ANYMO_DELTA[14:8]							0x00	R/W

Bit	Name	Function	Description
0x2B [7:0] 0x2C[14:8]	ANYMO_DELTA [14:0]	AnyMotion Delta Threshold	This unsigned delta count is the delta to detect motion activity.
0x2C [15]	**RESV**	Reserved	Reserved

Table 6-32: Register 0x2B, 0x2C bit assignments

MEMSIC

6.1.33 0X2D – ANYMOTION DURATION THRESHOLD

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x2D	**MOTION_ DUR Motion Duration**	ANYMO_DUR[7:0]								0x00	R/W

Bit	Name	Function	Description
0x2D [7:0]	ANYMO_DUR [7:0]	AnyMotion Duration Threshold	This unsigned value sets the minimum duration period (in samples) for a valid AnyMotion detection condition.

Table 6-33: Register 0x2D bit assignments

MEMSIC

6.1.34 0X2E – ANYMOTION CONTROL REGISTER 0

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x2E	**MOTION_ CTRL_0**	Motion Control Register 1	**RESV**	**RESV**	NO_MO_ ENABLE_Z	NO_MO_ ENABLE_Y	NO_MO_ ENABLE_X	ANYM_ ENABLE_Z	ANYM_ ENABLE_Y	ANYM_ ENABLE_X	0x00	R/W

Bit	Name	Function	Description
0	ANYM_ ENABLE_X	Enable/Disable AnyMotion activity detection on the X-axis.	0: Feature is disabled (default). 1: Feature is enabled.
1	ANYM_ ENABLE_Y	Enable/Disable AnyMotion activity detection on the Y-axis.	0: Feature is disabled (default). 1: Feature is enabled.
2	ANYM_ ENABLE_Z	Enable/Disable AnyMotion activity detection on the Z-axis.	0: Feature is disabled (default). 1: Feature is enabled.
3	NO_MO_ ENABLE_X	Enable/Disable NoMotion inactivity detection on the X-axis.	0: Feature is disabled (default). 1: Feature is enabled.
4	NO_MO_ ENABLE_Y	Enable/Disable NoMotion inactivity detection on the y-axis.	0: Feature is disabled (default). 1: Feature is enabled.
5	NO_MO_ ENABLE_Z	Enable/Disable NoMotion inactivity detection on the Z-axis.	0: Feature is disabled (default). 1: Feature is enabled.
6	**RESV**	Reserved	Reserved
7	**RESV**	Reserved	Reserved

Table 6-34: Register 0x2E bit assignments

6.1.35 0X2F – MOTION CONTROL REGISTER 1

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x2F	**MOTION_ CTRL_2**	Motion Control Register 2	**RESV**	TF_ ENABLE	SIXD_EN	**RESV**	SHAKE_EN	**RESV**	FREEFALL_ EN	TAP_EN	0x00	R/W

Bit	Name	Description
0	TAP_DTAP_EN	0: TAP/DTAP/TTAP detection is disabled (default). 1: TAP/DTAP/TTAP detection is enabled.
1	FREEFALL_EN	0: FREEFALL_EN detection is disabled (default). 1: FREEFALL_EN detection is enabled.
2	**RESV**	Reserved.
3	SHAKE_EN	0: Shake detection is disabled (default). 1: Shake detection is enabled.
4	**RESV**	Reserved.
5	SIXD_EN	0: SIXD (6D) detection is disabled (default). 1: SIXD (6D) detection is enabled.
6	TF_ENABLE	0: Tilt/Flip detection is disabled (default). 1: Tilt/Flip detection is enabled.
7	**RESV**	Reserved.

Table 6-35: Register 0x2F bit assignments

6.1.36 0X30 – MOTION CONTROL REGISTER 2

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x30	**MOTION_ CTRL_2**	Motion Control Register 2	MOTION_ RESET	**RESV**	**RESV**	**RESV**	**RESV**	RAW_ PROC_STAT	Z_AXIS_ORT	MOTION_ LATCH	0x00	R/W

Bit	Name	Description
0	MOTION_LATCH	0: Motion block does not latch outputs (default) 1: Motion block latches outputs
1	Z_AXIS_ORT	0: Z-axis orientation is positive through top of package. (default) 1: Z-axis orientation is positive through bottom of package. The Z-axis orientation tells the logic which way the packaged device is mounted. A value of '0' is used for a bottom mount, and '1' is used for a top mount (affects filt/flip detection). Note, this bit does not affect the polarity setting of the Z-axis, only with respect to the motion detection algorithms.
2	RAW_ PROC_STAT	0: Motion flag bits are filtered by debounce and other settings (default) 1: Motion flag bits provide real-time, raw motion information, useful for debug.
5:3	**RESV**	Reserved
6	**RESV**	Reserved
7	MOTION_ RESET	0: Motion block is not in reset (default) 1: The motion block is held in reset. SW must clear this bit for the reset to be released. This bit is not self-clearing.

Table 6-36: Register 0x30 bit assignments

6.1.37 0X31,0X32 – TILT/FLIP THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x31	**Tilt/Flip Threshold Register LSB**	TF_THR[7]	TF_THR[6]	TF_THR[5]	TF_THR[4]	TF_THR[3]	TF_THR[2]	TF_THR[1]	TF_THR[0]	0x00	R/W
0x32	**Tilt/Flip Threshold Register MSB**	**RESV**	TF_THR[14]	TF_THR[13]	TF_THR[12]	TF_THR[11]	TF_THR[10]	TF_THR[9]	TF_THR[8]	0x00	R/W

Bit	Name	Description
0x31[7:0] **0x32[14:8]**	TF_THR[14:0]	This value is used for both the Flat/Tilt/Flip algorithms TF_THR[14:0] is a 15-bit threshold value (unsigned) to detect Flat/Tilt/Flip position of the device. If the sample value is greater than the programmed value of this register, then a Tilt condition is detected. If the sample value is less than the programmed value of this register, then a Flat/Flip condition is detected depending on: • The sample value of the Z-axis. • The orientation of the chip is mounted on the platform which is determined by the Z-axis-orient bit at register 0x30 bit 1.

Table 6-37: Registers 0x31,0x32 bit assignments

MEMSIC

6.1.38 0X33 – TILT/FLIP DEBOUNCE REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x33	Tilt/Flip Debounce Register	TF_DB[7:0]								0x00	R/W

Bit	Name	Description
7:0	TF_DB[7:0]	Programmed debounce value to detect the Tilt/Flip condition and set the corresponding interrupt. Once a Tilt/Flip condition is detected for the duration programmed in this register, the Tilt/Flip interrupt is set. The debounce count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

Table 6-38: Register 0x33 bit assignments

MEMSIC

6.1.39 0X34,0X35 – NOMOTION THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x34	**NoMotion Threshold Register LSB**	NOMO_ THR[7]	NOMO_ THR[6]	NOMO_ THR[5]	NOMO_ THR[4]	NOMO_ THR[3]	NOMO_ THR[2]	NOMO_ THR[1]	NOMO_ THR[0]	0x00	R/W
0x35	**NoMotion Threshold Register MSB**	**RESV**	NOMO_ THR[14]	NOMO_ THR[13]	NOMO_ THR[12]	NOMO_ THR[11]	NOMO_ THR[10]	NOMO_ THR[9]	NOMO_ THR[8]	0x00	R/W

Bit	Name	Description
0x34[7:0] 0x35[14:8]	NOMO_THR[14:0]	This register holds the programmed 15-bit threshold value to detect No_Motion. If the delta of the current sample value and the previous sample value is less than the programmed value of this register, then NoMotion condition is detected.

Table 6-39: Register 0x34,0x35 bit assignments

MEMSIC

6.1.40 0X36 – NOMOTION DEBOUNCE REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x36	NoMotion Debounce Register	NOMO_DB[7:0]								0x00	R/W

Once a No_Motion condition is detected, the No_Motion interrupt is set in the interrupt register. This register holds the programmed debounce value to clear the No_Motion interrupt set in the interrupt register.

For the duration programmed in this register, if the No_Motion condition is not detected, then the No_Motion interrupt is cleared in the interrupt register. The debounce count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

MEMSIC

6.1.41 0X37,0X38 – SHAKE THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x37	Shake Threshold Register LSB	SH_THR[7:0]								0x00	R/W
0x38	Shake Threshold Register MSB	SH_THR[15:8]								0x00	R/W

This register holds the programmed 15-bit threshold value to detect Shake. If, the delta of the current sample value and the previous sample value, is greater than +/- programmed value of this register, then Shake condition is detected.

The threshold value is in terms of digital gain stage of the pipeline, prior to any range g-scale. For a 1.4fF/g sensitivity MEMS, this corresponds to a signed 15-bit, +/-24g reference frame of digital offset and gain corrected data.

MEMSIC

6.1.42 0X39,0X3A – SHAKE PEAK 2 PEAK DURATION THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x39	Peak P2P Duration Threshold LSB	PK_P2P_DUR[7]	PK_P2P_DUR[6]	PK_P2P_DUR[5]	PK_P2P_DUR[4]	PK_P2P_DUR[3]	PK_P2P_DUR[2]	PK_P2P_DUR[1]	PK_P2P_DUR[0]	0x00	R/W
0x3A	Peak P2P Duration Threshold MSB	RESV	SHK_CNT_DUR[2]	SHK_CNT_DUR[1]	SHK_CNT_DUR[0]	PK_P2P_DUR[11]	PK_P2P_DUR[10]	PK_P2P_DUR[9]	PK_P2P_DUR[8]	0x00	R/W

6.1.42.1 **PEAK AND PEAK_TO_PEAK DURATION**

This registers 0x39 and 0x3A[3:0] holds the programmed value to detect the Peak and the Peak to Peak width of the Shake.

If the sample value is beyond (+/-) the shake threshold, then a Peak is detected and its width is measured as defined in this register. If the sample value is within (+/-) the shake threshold, then a Peak to Peak is detected and its width is measured as defined in this register. The duration count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

6.1.42.2 **SHAKE COUNTER**

This register i.e. 0x3B[6:4] holds the programmed value of the number of shake cycles to be detect. Once the programmed number of shake cycles are detected, the Shake interrupt is set in the interrupt status register. The shake count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

MEMSIC

6.1.43 0X3B,0X3C – TAP EVENT THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x3B	TAP/DTAP/TTAP Event Threshold LSB Register	TAP_EVT_TH[7]	TAP_EVT_TH[6]	TAP_EVT_TH[5]	TAP_EVT_TH[4]	TAP_EVT_TH[3]	TAP_EVT_TH[2]	TAP_EV_TH[1]	TAP_EVT_TH[0]	0x00	R/W
0x3C	TAP/DTAP/TTAP Event Threshold MSB Register	**RESV**	TAP_EVT_TH[14]	TAP_EVT_TH[13]	TAP_EVT_TH[12]	TAP_EVT_TH[11]	TAP_EVT_TH[10]	TAP_EVT_TH[9]	TAP_EVT_TH[8]	0x00	R/W

This unsigned threshold value applies to all tap events (single, double, and triple tap). The threshold value is in term of the selected XL g-range.

Bit	Name	Function	Description
0x3B 7:0 **0x3C 6:0**	TAP_EVT_TH[14:0]	Tap Threshold Register	Specifies the threshold above which a tap event is detected. The value is a magnitude and is unsigned.

Table 6-40: Register 0x2A,0x2B bit assignments

MEMSIC

6.1.44 0X3D – TAP SHOCK DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x3D	TAP/DTAP/TTAP Shock Duration Register	TAP_SHOCK_DUR[7]	TAP_SHOCK_DUR[6]	TAP_SHOCK_DUR[5]	TAP_SHOCK_DUR[4]	TAP_SHOCK_DUR[3]	TAP_SHOCK_DUR[2]	TAP_SHOCK_DUR[1]	TAP_SHOCK_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	TAP_SHOCK_DUR[7:0]	Shock Duration Count for TAP/DTAP/TTAP	Specifies the shock duration in which the acceleration value should come below the tap event detection value . If the acceleration value does not fall below the event detection threshold in this period, then the event is not detected. The count is in terms of ODR/sample periods.

Table 6-41: Register 0x3D bit assignments

MEMSIC

6.1.45 0X3E – TAP QUIET DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x3E	TAP/DTAP/TTAP Quiet Duration Register	TAP_QUIET_DUR[7]	TAP_QUIET_DUR[6]	TAP_QUIET_DUR[5]	TAP_QUIET_DUR[4]	TAP_QUIET_DUR[3]	TAP_QUIET_DUR[2]	TAP_QUIET_DUR[1]	TAP_QUIET_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	TAP_ QUIET _DUR[7:0]	TAP/DTAP/TTAP Quiet Duration Register	After the shock period there should be no acceleration event above the detection threshold in Quiet Period. If there is an event above the threshold in Quiet Duration, then the tap event is not detected . This value is in terms of ODR or sample periods.

Table 6-42: Register 0x3E bit assignments

MEMSIC

6.1.46 0X3F – TAP LATENCY DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x3F	TAP Latency Duration Register LSB	TAP_LATENCY_DUR[7]	TAP_LATENCY_DUR[6]	TAP_LATENCY_DUR[5]	TAP_LATENCY_DUR[4]	TAP_LATENCY_DUR[3]	TAP_LATENCY_DUR[2]	TAP_LATENCY_DUR[1]	TAP_LATENCY_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	TAP_LATENCY_DUR[7:0]	Lower 8-bits of the Tap Latency Duration. The upper 5-bits are in register 0x2F.	Specifies the max delay between 2 successive tap events in generation of double tap and triple tap. This period starts after the quiet period is over the previous event. This value is in terms of ODR or sample periods.

Table 6-43: Register 0x3F bit assignments

MEMSIC

6.1.47 0X40 – TAP CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x40	Tap Control/TAP Latency Duration Register MSB	MASK_Z	MASK_Y	MASK_X	TAP_ LATENCY_DUR[12]	TAP_ LATENCY_DUR[11]	TAP_ LATENCY_ DUR[10]	TAP_ LATENCY_ DUR[9]	TAP_ LATENCY_ DUR[8]	0x00	R/W

Bit	Name	Function	Description
4:0	TAP_LATENCY_DUR[12:8]	Upper 5-bits of the Tap Latency Duration. The lower 8-bits are in register 0x44	Specifies the max delay between 2 successive tap events in generation of double tap and triple tap. This period starts after the quiet period is over the previous event. This value is in terms of ODR or sample periods.
5	MASK_X	Enable/Disable X-channel tap event detection	0: X channel tap detection enabled (default) 1: X channel tap detection disabled
6	MASK_Y	Enable/Disable Y-channel tap event detection	0: Y channel tap detection enabled (default) 1: Y channel tap detection disabled
7	MASK_Z	Enable/Disable Z-channel tap event detection	0: Z channel tap detection enabled (default) 1: Z channel tap detection disabled

Table 6-44: Register 0x40 bit assignments

MEMSIC

6.1.48 0X41,0X42 – FREEFALL THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x41	FreeFall Threshold LSB Register	FREEFALL_TH[7:0]								0x00	R/W
0x42	FreeFall Threshold MSB Register	RESV	FREEFALL_TH[14:8]							0x00	R/W

Bit	Name	Function	Description
0x41 7:0	FREEFALL_TH[7:0]	Lower 8-bits of the Tap Latency Duration. The upper 7-bits are in register 0x31	Specifies the threshold below which a freefall event is detected. All channel values need to be below this threshold for a freefall event to be detected.
0x42 6:0	FREEFALL_TH[14:8]	Upper 7-bits of the Tap Latency Duration. The lower 8-bits are in register 0x30.	
0x42 7	**RESV**	Reserved	Reserved

Table 6-45: Register 0x41,0x42 bit assignments

MEMSIC

6.1.49 0X43 – FREEFALL DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x43	FreeFall Duration Register	FREEFALL_DUR[7:0]								0x00	R/W

Bit	Name	Function	Description
7:0	FREEFALL_ DUR [7:0]	FreeFall Duration Count	The acceleration values for all 3 channels need to be below the freefall threshold value for at least the free fall duration for the event to be considered as a valid freefall event. This value is in terms of ODR or sample periods.

Table 6-46: Register 0x43 bit assignments

MEMSIC

6.1.50 0X44,0X45 – SIX DEGREES HIGH THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x44	SIXD High Threshold LSB Register	SIXD_HIGH_TH[7]	SIXD_HIGH_TH[6]	SIXD_HIGH_TH[5]	SIXD_HIGH_TH[4]	SIXD_HIGH_TH[3]	SIXD_HIGH_TH[2]	SIXD_HIGH_TH[1]	SIXD_HIGH_TH[0]	0x00	R/W
0x45	SIXD High Threshold MSB Register	**RESV**	SIXD_HIGH_TH[14]	SIXD_HIGH_TH[13]	SIXD_HIGH_TH[12]	SIXD_HIGH_TH[11]	SIXD_HIGH_TH[10]	SIXD_HIGH_TH[9]	SIXD_HIGH_TH[8]	0x00	R/W

Bit	Name	Function	Description
0x44[7:0]	SIXD_HIGH_TH [7:0]	Lower 8 bits of SIXD High Threshold LSB Register	Specifies the threshold above which an orientation event is detected. Two channels should have acceleration below the low threshold (SIXD_LOW_THRESH) and 1 channel should have acceleration above the threshold (SIXD_HIGH_THRESH) for the duration period (SIXD_DUR) to register an orientation change.
0x45 [6:0]	SIXD_HIGH_TH [14:8]	Upper 7 bits of SIXD High Threshold MSB Register	
0x45 [7]	**RESV**	Reserved	Reserved

Table 6-47: Register 0x44,0x45 bit assignments

MEMSIC

6.1.51 0X46,0X47 – SIX DEGREES LOW THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x46	SIXD Low Threshold LSB Register	SIXD_LOW_TH[7]	SIXD_LOW_TH[6]	SIXD_LOW_TH[5]	SIXD_LOW_TH[4]	SIXD_LOW_TH[3]	SIXD_LOW_TH[2]	SIXD_LOW_TH[1]	SIXD_LOW_TH[0]	0x00	R/W
0x47	SIXD Low Threshold MSB Register	**RESV**	SIXD_LOW_TH[14]	SIXD_LOW_TH[13]	SIXD_LOW_TH[12]	SIXD_LOW_TH[11]	SIXD_LOW_TH[10]	SIXD_LOW_TH[9]	SIXD_LOW_TH[8]	0x00	R/W

Bit	Name	Function	Description
0x46 [7:0]	SIXD_LOW_TH [7:0]	Lower 8 bits of SIXD Low Threshold LSB Register	Specifies the threshold below which an orientation event is detected. Two channels should have acceleration below the low threshold (SIXD_LOW_THRESH) and 1 channel should have acceleration above the threshold (SIXD_HIGH_THRESH) for the duration period (SIXD_DUR) to register an orientation change.
0x47[6:0]	SIXD_ LOW _TH [14:8]	Upper 7 bits of SIXD Low Threshold MSB Register	
0x47 [7]	**RESV**	Reserved	Reserved

Table 6-48: Register 0x46,0x47 bit assignments

MEMSIC

6.1.52 0X48 – SIX DEGREE DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x48	SIXD Duration Register	SIXD_DUR[7:0]								0x00	R/W

Bit	Name	Function	Description
0x37 [7:0]	SIXD_DUR [7:0]	8-bit duration value for SIXD evaluation	Two channels should have acceleration below the low threshold (SIXD_LOW_THRESH) and 1 channel should have acceleration above the threshold (SIXD_HIGH_THRESH) for the duration period (SIXD_DUR) to register an orientation change. This duration count is in terms of ODR or sample periods.

Table 6-49: Register 0x48 bit assignments

MEMSIC

6.1.53 0X49 – SIX DEGREES STATUS REGISTER

This read-only register reports the status of the SIXD orientation logic. Only one of the six bits below will be set to '1' at any time.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x49	SIXD Status Register	**RESV**	**RESV**	Z_NEG	Y_NEG	Z_NEG	Z_POS	Y_POS	X_POS	0x01	RO

Note that Motion register default values are set under XL power domain. It needs to enable XL_PWR_EN(Refer to register 0x02 bit0) and to disable hold/isolation cells(Refer to register 0x02 bit3) to get motion register default values.

Bit	Name	Function	Description
0	X_POS	X-axis positive	0: System is not in X_POS orientation 1 : System is in X_POS orientation
1	Y_POS	Y-axis positive	0: System is not in Y_POS orientation 1 : System is in Y_POS orientation
2	Z_POS	Z-axis positive	0: System is not in Z_POS orientation 1 : System is in Z_POS orientation
3	X_NEG	X-axis negative	0: System is not in X_NEG orientation 1 : System is in X_NEG orientation
4	Y_NEG	Y-axis negative	0: System is not in Y_NEG orientation 1 : System is in Y_NEG orientation
5	Z_NEG	Z-axis negative	0: System is not in Z_NEG orientation 1 : System is in Z_NEG orientation
6	**RESV**	Reserved	Reserved
7	**RESV**	Reserved	Reserved

Table 6-50: Register 0x49 bit assignments

6.1.54 0X4A – PIPELINE STATUS REGISTER

This read-only register reports the status of the XL pipeline.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x4A	**PIPELINE** Pileline Status Register	**RESV**				XL_CTRL_ TIMEOUT	PIPE_TIME OUT	PIPE_ STATE[1:0]		0x00	RO

Bit	Name	Function	Description
1:0	PIPE_STATE[1:0]	XL pipeline status.	0x0: PIPE_IDLE 0x1: PIPE_XY 0x2: PIPE_Z 0x3: Not used Status bits to report the activity of the XL pipeline.
2	PIPE_TIMEOUT	XL pipeline timeout status.	0: XL pipeline has not timed-out (default). 1: XL pipeline has timed out. The DIS_PIPE_TIMOUT control bit is in register 0x56 bit 0. The default pipeline timeout is 30 clock cycles. This is a debug bit.
3	XL_CTRL_TIMEOUT	XL Control FSM timeout status.	0: XL CTRL FSM has not timed-out (default). 1: XL CTRL FSM has timed-out. The XL_CTRL_TIMEOUT_EN control bit is in register 0x56 bit 2.
7:4	**RESV**	Reserved.	Reserved, returns ‘0’ when read.

Table 6-51: Register 0x4A bit assignments

6.1.55 0X4E-0X55 – XY AXIS LPF COEFFICIENTS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x4E	XL LPF Coefficient B0/B2 LSB	XY_LPF_B0[7]	XY_LPF_B0[6]	XY_LPF_B0[5]	XY_LPF_B0[4]	XY_LPF_B0[3]	XY_LPF_B0[2]	XY_LPF_B0[1]	XY_LPF_B0[0]	0x00	R/W
0x4F	XL LPF Coefficient B0 MSB	XY_LPF_B0[15]	XY_LPF_B0[14]	XY_LPF_B0[13]	XY_LPF_B0[12]	XY_LPF_B0[11]	XY_LPF_B0[10]	XY_LPF_B0[9]	XY_LPF_B0[8]	0x00	R/W
0x50	XL LPF Coefficient B1 LSB	XY_LPF_B1[7]	XY_LPF_B1[6]	XY_LPF_B1[5]	XY_LPF_B1[4]	XY_LPF_B1[3]	XY_LPF_B1[2]	XY_LPF_B1[1]	XY_LPF_B1[0]	0x00	R/W
0x51	XL LPF Coefficient B1 MSB	XY_LPF_B1[15]	XY_LPF_B1[14]	XY_LPF_B1[13]	XY_LPF_B1[12]	XY_LPF_B1[11]	XY_LPF_B1[10]	XY_LPF_B1[9]	XY_LPF_B1[8]	0x00	R/W
0x52	XL LPF Coefficient A1 LSB	XY_LPF_A1[7]	XY_LPF_A1[6]	XY_LPF_A1[5]	XY_LPF_A1[4]	XY_LPF_A1[3]	XY_LPF_A1[2]	XY_LPF_A1[1]	XY_LPF_A1[0]	0x00	R/W
0x53	XL LPF Coefficient A1 MSB	XY_LPF_A1[15]	XY_LPF_A1[14]	XY_LPF_A1[13]	XY_LPF_A1[12]	XY_LPF_A1[11]	XY_LPF_A1[10]	XY_LPF_A1[9]	XY_LPF_A1[8]	0x00	R/W
0x54	XL LPF Coefficient A2 LSB	XY_LPF_A2[7]	XY_LPF_A2[6]	XY_LPF_A2[5]	XY_LPF_A2[4]	XY_LPF_A2[3]	XY_LPF_A2[2]	XY_LPF_A2[1]	XY_LPF_A2[0]	0x00	R/W
0x55	XL LPF Coefficient A2 MSB	XY_LPF_A2[15]	XY_LPF_A2[14]	XY_LPF_A2[13]	XY_LPF_A2[12]	XY_LPF_A2[11]	XY_LPF_A2[10]	XY_LPF_A2[9]	XY_LPF_A2[8]	0x00	R/W

Bit	Name	Function	Description
0x4E 7:0 **0x4F 7:0**	XY LPF Coefficient B0/B2 LSB/MSB	16-bit value for LPF coefficient B0 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0x50 7:0 **0x51 7:0**	XY LPF Coefficient B1 LSB/MSB	16-bit value for LPF coefficient B1 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0x52 7:0 **0x53 7:0**	XY LPF Coefficient A1 LSB/MSB	16-bit value for LPF coefficient A1 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements. *This value is always considered a negative coefficient by the filter hardware.*
0x54 7:0 **0x55 7:0**	XY LPF Coefficient A2 LSB/MSB	16-bit value for LPF coefficient A2 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.

Table 6-52: Registers 0x4E-0x55 bit assignments

6.1.56 0X56 – PIPELINE CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x56	**PIPE_CTRL** PIPELINE Control Register	**RESV**				SDM_CLK_INV	XL_CTRL TIMEOU_EN	DIS_XL_AUTO_RESET	DIS_PIPE_TIMEOUT	0x04	RW

Bit	Name	Function	Description
0	DIS_PIPELINE_TIMEOUT	Disable pipeline timeout.	0: Pipeline timeout flag operates as normal (default). 1: Pipeline timeout flag is disabled. Note the pipeline timeout state flag is in register 0x4A bit 2.
1	DIS_XL_AUTO_RESET	Disable XL auto reset.	0: XL domain (wake domain) reset is applied (default). 1: XL domain (wake domain) reset is disabled. This bit is used to suppress the XL domain (wake domain) reset generated by the XL control logic when performing power management.
2	XL_CTRL_TIMEOUT_EN	Enable XL CTRL timeout.	0: XL_CTRL state machine timeout is disabled (default). 1: XL_CTRL state machine timeout is enabled. This feature prevents the XL_CTRL state machine from getting stuck in the SAMPLE_START state in WAKE mode. When the LPF reset is applied, there is a chance the XL pipeline will not send a “done” strobe to the XL_CTRL FSM and it will become non-responsive. Normally the SLEEP or STANDBY modes are required to recover, but the timeout feature will prevent this behavior in WAKE mode. Register 0x4A bit 3 reports if a timeout condition is detected.
3	SDM_CLK_INV	Invert the polarity of the clock used to Analog SDM.	0: Normal Analog SDM clk polarity (default). 1: Inverted Analog SDM clk polarity. This bit is intended to provide an option for Analog SDM/ADC. This bit changes the edge from positive (default) to negative. The clock applied to the Analog SDM is inverted.
7:4	**RESV**	Reserved.	Reserved, returns ‘0’ when read.

Table 6-53: Register 0x56 bit assignments

6.1.57 0X58 - 0X5D – XL OFFSET_0 REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x58	**XL_XOFF_0**	X_XOFF_0[7]	X_XOFF_0[6]	X_XOFF_0[5]	X_XOFF_0[4]	X_XOFF_0[3]	X_XOFF_0[2]	X_XOFF_0[1]	X_XOFF_0[0]	OTP	R/W
0x59	**XL_XOFF_0**	X_XOFF_0[15]	X_XOFF_0[14]	X_XOFF_0[13]	X_XOFF_0[12]	X_XOFF_0[11]	X_XOFF_0[10]	X_XOFF_0[9]	X_XOFF_0[8]	OTP	R/W
0x5A	**XL_YOFF_0**	X_YOFF_0[7]	X_YOFF_0[6]	X_YOFF_0[5]	X_YOFF_0[4]	X_YOFF_0[3]	X_YOFF_0[2]	X_YOFF_0[1]	X_YOFF_0[0]	OTP	R/W
0x5B	**XL_YOFF_0**	X_XOFF_0[15]	X_YOFF_0[14]	X_YOFF_0[13]	X_YOFF_0[12]	X_YOFF_0[11]	X_YOFF_0[10]	X_YOFF_0[9]	X_YOFF_0[8]	OTP	R/W
0x5C	**XL_ZOFF_0**	X_ZOFF_0[7]	X_ZOFF_0[6]	X_ZOFF_0[5]	X_ZOFF_0[4]	X_ZOFF_0[3]	X_ZOFF_0[2]	X_ZOFF_0[1]	X_ZOFF_0[0]	OTP	R/W
0x5D	**XL_ZOFF_0**	X_XOFF_0[15]	X_ZOFF_0[14]	X_ZOFF_0[13]	X_ZOFF_0[12]	X_ZOFF_0[11]	X_ZOFF_0[10]	X_ZOFF_0[9]	X_ZOFF_0[8]	OTP	R/W

Note, these offset settings are applied when register 0x20 bit 4 = ‘0’.

Bit	Name	Function	Description
0x58 7:0 **0x59 7:0**	XL X-axis Offset LSB/MSB	X-axis, pipeline digital offset adjustment	This is a signed 2’s complement 16-bit value applied as an offset adjustment to the corresponding XL channel. Digital offset can range from 0x8000 (-32K) to 0x7FFF (+32K).
0x5A 7:0 **0x5B 7:0**	XL Y-axis Offset LSB/MSB	Y-axis, pipeline digital offset adjustment	This is a signed 2’s complement 16-bit value applied as an offset adjustment to the corresponding XL channel. Digital offset can range from 0x8000 (-32K) to 0x7FFF (+32K).
0x5C 7:0 **0x5D 7:0**	XL Z-axis Offset LSB/MSB	Z-axis, pipeline digital offset adjustment	This is a signed 2’s complement 16-bit value applied as an offset adjustment to the corresponding XL channel. Digital offset can range from 0x8000 (-32K) to 0x7FFF (+32K).

Table 6-54: Register 0x58-0x5D bit assignments

6.1.58 0X5E - 0X61,0X6C,0X79 – XL OFFSET_1 REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x5E	**XL_XOFF_1**	X_XOFF_1[7]	X_XOFF_1[6]	X_XOFF_1[5]	X_XOFF_1[4]	X_XOFF_1[3]	X_XOFF_1[2]	X_XOFF_1[1]	X_XOFF_1[0]	OTP	R/W
0x5F	**XL_XOFF_1**	X_XOFF_1[15]	X_XOFF_1[14]	X_XOFF_1[13]	X_XOFF_1[12]	X_XOFF_1[11]	X_XOFF_1[10]	X_XOFF_1[9]	X_XOFF_1[8]	OTP	R/W
0x60	**XL_YOFF_1**	X_YOFF_1[7]	X_YOFF_1[6]	X_YOFF_1[5]	X_YOFF_1[4]	X_YOFF_1[3]	X_YOFF_1[2]	X_YOFF_1[1]	X_YOFF_1[0]	OTP	R/W
0x61	**XL_YOFF_1**	X_XOFF_1[15]	X_YOFF_1[14]	X_YOFF_1[13]	X_YOFF_1[12]	X_YOFF_1[11]	X_YOFF_1[10]	X_YOFF_1[9]	X_YOFF_1[8]	OTP	R/W
0x6C	**XL_ZOFF_1**	X_ZOFF_1[7]	X_ZOFF_1[6]	X_ZOFF_1[5]	X_ZOFF_1[4]	X_ZOFF_1[3]	X_ZOFF_1[2]	X_ZOFF_1[1]	X_ZOFF_1[0]	OTP	R/W
0x79	**XL_ZOFF_1**	X_XOFF_1[15]	X_ZOFF_1[14]	X_ZOFF_1[13]	X_ZOFF_1[12]	X_ZOFF_1[11]	X_ZOFF_1[10]	X_ZOFF_1[9]	X_ZOFF_1[8]	OTP	R/W

Note, these offset settings are applied when register 0x20 bit 4 = ‘1’.

Bit	Name	Function	Description
0x5E 7:0 **0x5F 7:0**	XL X-axis Offset LSB/MSB	X-axis, pipeline digital offset adjustment	This is a signed 2’s complement 16-bit value applied as an offset adjustment to the corresponding XL channel. Digital offset can range from 0x8000 (-32K) to 0x7FFF (+32K).
0x60 7:0 **0x61 7:0**	XL Y-axis Offset LSB/MSB	Y-axis, pipeline digital offset adjustment	This is a signed 2’s complement 16-bit value applied as an offset adjustment to the corresponding XL channel. Digital offset can range from 0x8000 (-32K) to 0x7FFF (+32K).
0x6C 7:0 **0x79 7:0**	XL Z-axis Offset LSB/MSB	Z-axis, pipeline digital offset adjustment	This is a signed 2’s complement 16-bit value applied as an offset adjustment to the corresponding XL channel. Digital offset can range from 0x8000 (-32K) to 0x7FFF (+32K).

Table 6-55: Register 0x5E-0x61,0x6C,0x79 bit assignments

6.1.59 0X62 – XL POLARITY REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x62	**XL Polarity Register**	I2C_ ADDR_1	I2C_ ADDR_0	**RESV**	**RESV**	**RESV**	XL_ Z_POL	XL_ Y_POL	XL_ X_POL	OTP	R/W

The polarity control for each channel is at the end of the XL pipeline. When an axis is inverted, the output data is 2's complemented.

Bit	Name	Function	Description
0	XL_X_POL	X-axis polarity	0: X-axis data is not-inverted at end of pipeline (default) 1: X-axis data is not-inverted at end of pipeline.
1	XL_Y_POL	Y-axis polarity	0: Y-axis data is not-inverted at end of pipeline (default) 1: Y-axis data is not-inverted at end of pipeline.
2	XL_Z_POL	Z-axis polarity	0: Z-axis data is not-inverted at end of pipeline (default) 1: Z-axis data is not-inverted at end of pipeline.
3	**RESV**	Reserved	Reserved.
4	**RESV**	Reserved	Reserved.
5	**RESV**	Reserved	Reserved.
6	I2C_ADDR_0	I2C slave address bit 0	0: Bit 0 of the 7-bit I2C slave address is 0 (default). 1: Bit 0 of the 7-bit I2C slave address is 1. See Table 8 for available slave IDs.
7	I2C_ADDR_1	I2C slave address bit 1	0: Bit 1 of the 7-bit I2C slave address is 0 (default). 1: Bit 1 of the 7-bit I2C slave address is 1. See Table 8 for available slave IDs.

Table 6-56: Register 0x62 bit assignments

6.1.60 0X63-0X69 – XL AOFS OFFSET REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x63	**AOFS_XP**	AOFS_XP[7:0]								OTP	R/W
0x64	**AOFS_XP**	AOFS_XN[7:0]								OTP	R/W
0x65	**AOFS_YP**	AOFS_YP[7:0]								OTP	R/W
0x66	**AOFS_YN**	AOFS_YN[7:0]								OTP	R/W
0x67	**AOFS_ZP**	AOFS_ZP[7:0]								OTP	R/W
0x68	**AOFS_ZN**	AOFS_ZN[7:0]								OTP	R/W
0x69	**AOFS_MSB/ PREGAIN_MSB**	PRE_ DGAIN_Z[8]	PRE_ DGAIN_Y[8]	PRE_ DGAIN_X[8]	**RESV**	AOFSN_Y[8]	AOFSP_Y[8]	AOFSN_X[8]	AOFSP_X[8]	OTP	R/W

Bit	Name	Function	Description
0x63 [7:0] 0x69 [0]	AOFS_XP[8:0]	9-bit analog offset adjustment value for XP side of X-axis MEMS input.	9-bit unsigned value, 0x000 to 0x1FF (0 to 511). The total AOFS capacitance is: **Caofs = 2 fF * (28 + aofs[8:0])**
0x64 [7:0] 0x69 [1]	AOFS_XN[8:0]	9-bit analog offset adjustment value for XN side of X-axis MEMS input.	
0x65 [7:0] 0x69 [2]	AOFS_YP[8:0]	9-bit analog offset adjustment value for YP side of Y-axis MEMS input.	
0x66 [7:0] 0x69 [3]	AOFS_YN[8:0]	9-bit analog offset adjustment value for YN side of Y-axis MEMS input.	
0x67 [7:0]	AOFS_ZP[7:0]	8-bit analog offset adjustment value for ZP side of Z-axis MEMS input.	
0x68 [7:0]	AOFS_ZN[7:0]	8-bit analog offset adjustment value for ZN side of Z-axis MEMS input.	

Table 6-57: Register 0x63-0x69 bit assignments

6.1.61 0X6A,0X6B – XL ANALOG GAIN REGISTER 1 AND 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x6A	**XL Analog Gain Register 1**	ACL_AGAIN_Y[3:0]				ACL_AGAIN_X[3:0]				OTP	R/W
0x6B	**XL Analog Gain Register 2**	HYSTERESIS_HIGH	EN_IO_FILT_ I3C_CTRL	EN_IO_ FILT_VALUE	STICTION_EN	ACL_AGAIN_Z[3:0]				OTP	R/W

Bit	Name	Function	Description
3:0	ACL_AGAIN_X[3:0]	Select the analog gain (AFG) for the X-axis.	0x0: SDM FS = 5fF 0x1: SDM FS = 10fF 0x2: SDM FS = 15fF 0x3: SDM FS = 20 fF 0x4: SDM FS = 25 fF 0x5: SDM FS = 30 fF 0x6: SDM FS = 35 fF 0x7: SDM FS = 40 fF 0x8: SDM FS = 45 fF 0x9: SDM FS = 50 fF 0xA: SDM FS = 55 fF 0xB: SDM FS = 60 fF 0xC: SDM FS = 65 fF 0xD: SDM FS = 70 fF 0xE: SDM FS = 75 fF 0xF: SDM FS = 80 fF gsel mode: SDM FS = 110 fF **(note special gsel mode)** **Ctotal = 5 fF * (1 + ACL_AGAIN[3:0])**
7:4	ACL_AGAIN_Y[3:0]	Select the analog gain (AFG) for the Y-axis.	

Table 6-58: Register 0x6A bit assignments

MEMSIC

Bit	Name	Function	Description
2:0	ACL_AGAIN_Z[3:0]	Select the analog gain (AFG) for the Z-axis.	0x0: SDM FS = 5fF 0x1: SDM FS = 10fF 0x2: SDM FS = 15fF 0x3: SDM FS = 20 fF 0x4: SDM FS = 25 fF 0x5: SDM FS = 30 fF 0x6: SDM FS = 35 fF 0x7: SDM FS = 40 fF 0x8: SDM FS = 45 fF 0x9: SDM FS = 50 fF 0xA: SDM FS = 55 fF 0xB: SDM FS = 60 fF 0xC: SDM FS = 65 fF 0xD: SDM FS = 70 fF 0xE: SDM FS = 75 fF 0xF: SDM FS = 80 fF gsel mode: SDM FS = 110 fF **(note special gsel mode)** **Ctotal = 5 fF * (1 + ACL_AGAIN[3:0])**
4	STICTION_EN	Enable the XL stiction detection/recovery feature.	0: Stiction detection and recovery is not enabled (default). 1: Stiction detection and recovery is enabled. This OTP bit allows the stiction detection/recovery feature to be disabled or enable for customer parts.
5	EN_IO_FILT_VALUE	Select state of IO filter when manual control is enabled.	0: IO filter is disabled for SCL and SDA input paths. 1: IO filter is enabled for SCL and SDA input paths.
6	EN_IO_FILT_I3C_CTRL	Enable manual IO filter control.	0: Manual control is disabled. (default). 1: Manual control is enabled.
7	HYSTERESIS_HIGH	Enable higher Vih level for digital inputs.	0: High-level hysteresis is not enabled (default). 1: High-level hysteresis is enabled.

Table 6-59: Register 0x6B bit assignments

6.1.61.1 RECOMMENDED AFG VS MEMS SENSITIVITY

Sensitivity	Full Scale 24g	AFG (Analog Gain)
<0.2fF/G	<5fF	0 (5fF)
<0.4fF/G	<10fF	1 (10fF)
<0.6fF/G	<15fF	2 (15fF)
<0.8fF/G	<20fF	3 (20fF)
<1.0fF/G	<25fF	4 (25fF)
<1.25fF/G	<30fF	5 (30fF)
<1.45fF/G	<35fF	6 (35fF)
<1.65fF/G	<20fF	7 (40fF)
<1.875fF/G	<45fF	8 (45fF)
<2.0fF/G	<50fF	9 (50fF)
<2.29fF/G	<55fF	10 (55fF)
<2.5fF/G	<60fF	11 (60fF)
<2.7fF/G	<65fF	12 (65fF)
<2.9fF/G	<70fF	13 (70fF)
<3.125fF/G	<75fF	14 (75fF)
<3.33fF/G	<80fF	15 (80fF)

Table 6-60: MEMS sensitivity vs analog gain

If the MEMS sensitivity is higher than 3.33fF/G, the full scale of the ASIC may not be sufficient to reach 16G full range.

6.1.62 0X6D-0X72 – TCO COEFFICIENT REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x6D	**XL_X_TCO_A1 Coefficient**	GAIN_SHIFT_X[0]	XL_X_TCO_A1[6:0]							OTP	R/W
0x6E	**XL_X_TCO_A2 Coefficient**	GAIN_SHIFT_X[1]	XL_X_TCO_A2[6:0]							OTP	R/W
0x6F	**XL_Y_TCO_A1 Coefficient**	GAIN_SHIFT_X[2]	XL_Y_TCO_A1[6:0]							OTP	R/W
0x70	**XL_Y_TCO_A2 Coefficient**	GAIN_SHIFT_X[3]	XL_Y_TCO_A2[6:0]							OTP	R/W
0x71	**XL_Z_TCO_A1 Coefficient**	GAIN_SHIFT_X[4]	XL_Z_TCO_A1[6:0]							OTP	R/W
0x72	**XL_Z_TCO_A2 Coefficient**	GAIN_SHIFT_X[5]	XL_Z_TCO_A2[6:0]							OTP	R/W

Bit	Name	Function	Description
6:0	**XL_X_TCO_A1** **XL_Y_TCO_A1** **XL_Z_TCO_A1**	First order coefficient 'A1' for X, Y, and Z	Range: -64 to +63 (0x40 to 0x3F, 2's complement) Fixed point scale is 2^3.
6:0	**XL_X_TCO_A2** **XL_Y_TCO_A2** **XL_Z_TCO_A2**	Second order coefficient 'A2' for X, Y, and Z	Range: -64 to +63 (0x40 to 0x3F, 2's complement) Fixed point scale is 2^9.

Table 6-61: TCO coefficients

Atria2_TCO								
	a2				a1			
	Suggest	Fixed point	Power index	bits	Suggest	Fixed point	Power index	bits
Max	0.1365	0.125	2^-3	7	6.8266	8	2^3	7
Min	-0.1365	-0.125	2^-3		-6.8266	-8	2^3	
Step	0.004265625	0.001953125	2^-9		0.21333125	0.125	2^-3	

Table 6-62: Format and range of TCO coefficients

The TCO correction applied to the XL output data is represented by the following:

$$\boldsymbol{data_{tco} = data + A2 * (T - T0)^2 + A1 * (T - T0)}$$

T0: Factory trim temperature stored in OTP.

T: Current temperature from the temperature sensor:

A1: Coefficient 'A' from the table above.

A2: Coefficient 'A' from the table above.

data: Output data from the corresponding X, Y, Z channel.

$data_{tco}$: TCO corrected data from the corresponding X, Y, Z channel.

See section 6.1.63.2 for the fine sensitivity gain trim.

Bits	Name	Function	Description
0x6D[7] **0x6E[7]** **0x6F[7]** **0x70[7]** **0x71[7]** **0x72[7]**	**GAIN_SHIFT_X[5:0]**	Gain shift factor for X-channel. Used to compensate for changes in sensitivity when changing SDM sampling frequency.	Parameter range: 0x20: -32 0x00: 0 (default) 0x1F: +31

Table 6-63: Format for X-axis gain shift

Step(fixed-pointed)	Step float	Parameter range	Trim range
1/512	0.1953%	-32~31 (6 bits)	-6%~6%

$$N_{output} = \left(input * \frac{40+PRE_{GAIN}}{128} + doffset + tco\right) * \left(1 + \frac{Gain_{shift}}{512}\right) * \left(1 + \frac{tcs}{8192}\right)$$

Focus on:

$$A = \left(1 + \frac{Gain_{shift}}{512}\right) * \left(1 + \frac{tcs}{8192}\right) = 1 + \frac{Gain_{shift}}{512} * \frac{tcs}{8192} + \frac{16Gain_{shift} + tcs}{8192}$$

$$\approx 1 + \frac{16Gain_{shift} + tcs}{8192}$$

6.1.63 0X73-0X78 – TCS COEFFICIENT REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x73	**XL_X_TCS_A1 Coefficient**	GAIN_SHIFT_Y[1]	GAIN_SHIFT_Y[0]	XL_X_TCS_A1[5:0]						OTP	R/W
0x74	**XL_X_TCS_A2 Coefficient**	GAIN_SHIFT_Y[3]	GAIN_SHIFT_Y[2]	XL_X_TCS_A2[5:0]						OTP	R/W
0x75	**XL_Y_TCS_A1 Coefficient**	GAIN_SHIFT_Y[5]	GAIN_SHIFT_Y[4]	XL_Y_TCS_A1[5:0]						OTP	R/W
0x76	**XL_Y_TCS_A2 Coefficient**	GAIN_SHIFT_Z[1]	GAIN_SHIFT_Z[0]	XL_Y_TCS_A2[5:0]						OTP	R/W
0x77	**XL_Z_TCS_A1 Coefficient**	GAIN_SHIFT_Z[3]	GAIN_SHIFT_Z[2]	XL_Z_TCS_A1[5:0]						OTP	R/W
0x78	**XL_Z_TCS_A2 Coefficient**	GAIN_SHIFT_Z[5]	GAIN_SHIFT_Z[4]	XL_Z_TCS_A2[5:0]						OTP	R/W

6.1.63.1 TCS COEFFICIENTS

Bit	Name	Function	Description
5:0	**XL_X_TCS_A1** **XL_Y_TCS_A1** **XL_Z_TCS_A1**	First order coefficient 'A1' for X, Y, and Z	See table below.
5:0	**XL_X_TCS_A2** **XL_Y_TCS_A2** **XL_Z_TCS_A2**	Second order coefficient 'A2' for X, Y, and Z	See table below.

Table 6-64: TCS coefficients

(1) Compensation formula: TCS = a2(T-T_0)^2 + a1(T-T_0).
   a) Coefficients: secondary term coefficient a2, Primary term coefficient a1.
   b) Room temperature T_0, typical value is 25 degrees Celsius.
   c) Temperature variable T, typical range -40 to 85 degrees Celsius.

$$y_{sensitivity}(T) = y_{sensitivity}(T0)(1 + y_{TCS}(T))$$

$$y_{TCS}(T) = \mathbf{a_2} * (\mathbf{T} - \mathbf{T0})^{\mathbf{2}} + \mathbf{a_1} * (\mathbf{T} - \mathbf{T0}))$$

where:

$y_{sensitivity}(T)$: **sensitivity deviation at temperature T**

$y_{sensitivity}(T0)$: **sensitivity deviation at temperature T0**

$y_{TCS}(T)$: **Temperature coefficient of Sensitivity(TCS), can be represented by a 2nd order polynomial**

Atria2_TCS								
	a2(the second order)				a1(the first order)			
	Suggest	Fixed point	Power index	bits	Suggest	Fixed point	Power index	bits
Max	0.000005	7.63E-06	2^-17	6	0.0005	4.88E-04	2^-11	6
Min	-0.000005	-7.63E-06	2^-17		-0.0005	-4.88E-04	2^-11	
Step	3.125E-07	2.38E-07	2^-22		3.13E-05	1.53E-05	2^-15	

Table 6-65: Format and range of TCS coefficients

MEMSIC

6.1.63.2 FINE SENSITIVITY GAIN TRIM

Bits	Name	Function	Description
0x73[7:6] **0x74[7:6]** **0x75[7:6]**	**GAIN_SHIFT_Y[5:0]**	Gain shift factor for Y-channel. Used to compensate for changes in sensitivity when changing SDM sampling frequency.	Parameter range: 0x20: -32 0x00: 0 (default) 0x1F: +31
0x76[7:6] **0x77[7:6]** **0x78[7:6]**	**GAIN_SHIFT_Z[5:0]**	Gain shift factor for Z-channel. Used to compensate for changes in sensitivity when changing SDM sampling frequency.	

Table 6-66: Y and z gain shift assignments

Step(fixed-pointed)	Step float	Parameter range	Trim range
1/512	0.1953%	-32~31 (6 bits)	-6%~6%

$$N_{output} = \left(input * \frac{40+PRE_{GAIN}}{128} + doffset + tco\right) * \left(1 + \frac{Gain_{shift}}{512}\right) * \left(1 + \frac{tcs}{8192}\right)$$

Focus on:

$$A = \left(1 + \frac{Gain_{shift}}{512}\right) * \left(1 + \frac{tcs}{8192}\right) = 1 + \frac{Gain_{shift}}{512} * \frac{tcs}{8192} + \frac{16Gain_{shift} + tcs}{8192}$$

$$\approx 1 + \frac{16Gain_{shift} + tcs}{8192}$$

Trim Procedure

(1)Set sys_clk to 1.6MHz, and set *offset_sel to 1, read out rbm_1g and rbm_-1g, and calculate gain_float1 and offset_float1;*

*(2) set **OTP_OFFSET1** to **round(offset_float1)**, set **OTP_PREGAIN** to **round(gain_float1*128-40)**;*

(3) set sys_clk to 200KHz, and set offset_sel to 0, read out rbm_1g and rbm_-1g, and calculate gain_float2 and offset_float2;

*(4) set **OTP_OFFSET0** to **round(offset_float2)**, set **OTP_GAINSHIFT** to **round((gain_float2/gain_float1-1)*512)**;*

6.1.64 0X7A,0X7B,0X7C,0X7D – TEMPERATURE TRIM REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x7A	TEMP_DATA_T0_LSB	Factory Trim Temp T0 Data LSB	TEMP_DATA_T0[7:0]								OTP	R/W
0x7B	TEMP_DATA_T0_MSB	Factory Trim Temp T0 Data MSB	PCODE[0]	TEMP_COEFF[8]	TEMP_TRIM_T0[2:0]			TEMP_DATA_T0 [10:8]			OTP	R/W
0x7C	TEMP_TRIM_T0	Factory Trim Temp T0	TEMP_TRIM_T0[10:3]								OTP	R/W
0x7D	TEMP_COEFF	Temperature Coefficient	TEMP_COEFF[7:0]								OTP	R/W

Bit	Name(s)	Function	Description
0x7A [7:0] **0x7B [2:0]**	TEMP_DATA_T0[10:0] **code(T0)** **or code_T0**	Output code (data) of the temperature sensor at the trim temperature of T0.	This 11-bit value is the output of temperature sense @ T0 at which the factory trim was performed. Range: 800 - 1400
0x7B [5:3] **0x7C [7:0]**	TEMP_TRIM_T0[10:0] **T0** **or temp_T0**	Temperature at which factory trim was performed, T0.	This 11-bit value is the temperature T0 at which the factory trim was performed. Range: 293 - 303
0x7B [7:0] **0x7B [6]**	TEMP_COEFF[8:0] **GC1 or** **gcoef**	Temperature scaling coefficient.	Temperature scaling coefficient. Range: 200 - 500
0x7B [7]	PCODE[0]	Optional product code.	Bit 0 of 3-bit PCODE, used for SW identification of specific Memsic product splits based on a common CMOS version.

Table 6-67: Registers 0x7A,0x7B,0x7C,0x7D bit assignments

The temperature sensor output is reported in registers 0x0E and 0x0F. The output temperature is clamped between 223 and 398 kelvin. The corrected temperature is represented by

$$\boldsymbol{T} = \frac{\frac{\boldsymbol{code(T0)}}{\boldsymbol{code(T)}} - \boldsymbol{1}}{\boldsymbol{TC1}} + \boldsymbol{T0} = \boldsymbol{GC1} * \left(\frac{\boldsymbol{code(T0)}}{\boldsymbol{code(T)}} - \boldsymbol{1} \right) + \boldsymbol{T0}$$

$T0$: calibration temperature

$code(T0)$: temperature sensor output code (11-bit) at calibration temperature $T0$

$code(T)$: temperature sensor output code (11-bit) at temperature T

$TC1$: linear fit coefficient

$GC1$: $GTC1=1/TC1$ (9-bit)

T: current temperature (11-bit)

MEMSIC

6.1.65 0X7E,0X7F,0X80 - PRE-DIGITAL GAIN REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x7E	PRE_ DGAIN_X	X-axis Pre Digital Gain	PRE_GAIN_X[7:0]								OTP	R/W
0x7F	PRE_ DGAIN_Y	Y-axis Pre Digital Gain	PRE_GAIN_Y[7:0]								OTP	R/W
0x80	PRE_ DGAIN_Z	Z-axis Pre Digital Gain	PRE_GAIN_Z[7:0]								OTP	R/W
0x69	PREGAIN_ MSB	XYZ Pre-Digital Gain MSB	PRE_ DGAIN_ Z[8]	PRE_ DGAIN_ Y[8]	PRE_ DGAIN_ X[8]	**RESV**	AOFSN_ Y[8]	AOFSP_ Y[8]	AOFSN_ X[8]	AOFSP _X[8]	OTP	R/W

Bit	Name	Function	Description
0x69[5], 0x7E [7:0]	PRE_GAIN_X[8:0]	Pre-digital gain for X-axis.	9-bit unsigned pre (first) digital gain stage for XL. Range = 0.3125 to 4.26875 Use a value of 44 to set the pre-gain to 1x. PRE_DGAIN = (20 + PRE_GAIN_CODE) / 64
0x69[6], 0x7F [7:0]	PRE_GAIN_Y[8:0]	Pre-digital gain for Y-axis.	
0x69[7], 0x80 [7:0]	PRE_GAIN_Z[8:0]	Pre-digital gain for Z-axis.	

Table 6-68: Registers 0x69,0x7E,0x7F,0x80 bit assignments

MEMSIC

6.1.66 0X81,0X82 - SYS_OSC TRIM REGISTERS 1/2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x81	**SYS_OSC Trim Register 1**	PCODE[1]	SYS_OSC_ FTRIM1[6]	SYS_OSC_ FTRIM1[5]	SYS_OSC_ FTRIM1[4]	SYS_OSC_ FTRIM1[3]	SYS_OSC_ FTRIM1[2]	SYS_OSC_ FTRIM1[1]	SYS_OSC_ FTRIM1[0]	OTP	R/W
0x82	**SYS_OSC Trim Register 2**	PCODE[2]	SYS_OSC_ FTRIM2[6]	SYS_OSC_ FTRIM2[5]	SYS_OSC_ FTRIM2[4]	SYS_OSC_ FTRIM2[3]	SYS_OSC_ FTRIM2[2]	SYS_OSC_ FTRIM2[1]	SYS_OSC_ FTRIM1[0]	OTP	R/W

Bit	Name	Function	Description
0x81 [6:0]	SYS_OSC_FTRIM1	7-bit trim for the SYS_OSC. **Applies to 1.6 MHz mode.**	This value is OTP backed and reloaded on a POR or soft-reset. This value is unsigned. When the SYS_OSC is in 1.6 MHz mode (0x20 [6] = '0') this trim value is used to adjust the SYS_OSC. 0x00: Lowest trim value (default). 0x40: Mid-range trim value **0x50: Default value while POR or BOOT is in progress.** 0x7F: Highest trim value.
0x81 [7]	PCODE[1]	Optional product code.	Bit 1 of 3-bit PCODE, used for SW identification of specific Memsic product splits based on a common CMOS version.

Table 6-69: Register 0x81 bit assignments

Bit	Name	Function	Description
0x82 [6:0]	SYS_OSC_FTRIM2	7-bit trim for the SYS_OSC. **Applies to 200 kHz mode.**	This value is OTP backed and reloaded on a POR or soft-reset. This value is unsigned. When the SYS_OSC is in 200 kHz mode (0x20 [6] = '1') this trim value is used to adjust the SYS_OSC. 0x00: Lowest trim value (default). 0x40: Mid-range trim value 0x7F: Highest trim value.
0x82 [7]	PCODE[2]	Optional product code.	Bit 2 of 3-bit PCODE, used for SW identification of specific Memsic product splits based on a common CMOS version.

Table 6-70: Register 0x82 bit assignments

6.1.67 0X84 - 0X87 – DEVICE ID/PART ID REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x84	**Part ID Byte 1**	PID_1[7]	PID_1[6]	PID_1[5]	PID_1[4]	PID_1[3]	PID_1[2]	PID_1[1]	PID_1[0]	OTP	R/W
0x85	**Part ID Byte 2**	PID_2[7]	PID_2[6]	PID_2[5]	PID_2[4]	PID_2[3]	PID_2[2]	PID_2[1]	PID_2[0]	OTP	R/W
0x86	**Part ID Byte 3**	PID_3[7]	PID_3[6]	PID_3[5]	PID_3[4]	PID_3[3]	PID_3[2]	PID_3[1]	PID_3[0]	OTP	R/W
0x87	**Part ID Byte 4**	PID_4[7]	PID_4[6]	PID_4[5]	PID_4[4]	PID_4[3]	PID_4[2]	PID_4[1]	PID_4[0]	OTP	R/W

The Atria2 part ID (serial number) is stored in these four dedicated OTP backed registers. The recommended format is:

Addr	Name	Description
0x84	PID_1[7:0]	Device X-location on the wafer.
0x85	PID_2[7:0]	Device Y-location on the wafer.
0x86	PID_3[7:0]	Wafer ID.
0x87	PID_4[7:0]	Lot ID.

Table 6-71: Register 0x84-0x87 suggested assignments

MEMSIC

6.1.68 0X88 - ANALOG CONTROL REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x88	ANA_CTRL_1 Analog Control Register 1	RESV			PM_IBIAS_PD_EN	PM_ALDO_PD_EN	PMU_IBIAS_PD	RESV	PMU_AVDD_PD	0x00	R/W

Bit	Name	Function	Description
0	PMU_AVDD_PD	Manual control for powering down analog and ALDO.	0: Manual control of ALDO/AVDD power is disabled (default). 1: Force the ALDO/AVDD to power down. The PMU_AVDD_PD control is affected by: -0x88[0] state -Automatic power control (if enabled) -SLEEP Mode (ALDO is powered off)
1	RESV	Reserved.	Reserved. Note, was connected to PMU_BG_LP. No longer connected in the analog block.
2	PMU_IBIAS_PD	Manual control for powering down the IBIAS/current in the analog.	0: Manual control of IBIAS block power is disabled. 1: Force the IBIAS block to power down. The PMU_IBIAS_PD control is affected by: -0x88[2] state -Automatic power control (if enabled) -SLEEP Mode (IBIAS is powered off)
3	PM_ALDO_PD_EN	Allow the ALDO to be powered off when in duty cycling mode.	0: The ALDO/AVDD is not powered off between duty-cycled samples (default). 1: The ALDO/AVDD is powered off between duty-cycled samples. Note that register 0x05 bit 3 must be set to '1' for this mode to work.
4	PM_IBIAS_PD_EN	Allow the IBIAS/currents to be powered off when in duty cycling mode.	0: The IBIAS block is not powered off between duty-cycled samples (default). 1: The IBIAS block is powered off between duty-cycled samples. Note that register 0x05 bit 3 must be set to '1' for this mode to work.
7:5	RESV	Reserved.	Reserved. Note, was PMU_ALDO_IB_N[2:0], no longer connected in the analog block.

Table 6-72: Register 0x88 bit assignments

6.1.69 0X8C – ANALOG CONTROL REGISTER 5

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x8C	**ANA_CTRL_5 Analog Control Register 5**	PMU_ALDO_STB_BOOST	PMU_DLDO_STB_BOOST	LP_MODE_OTA2_Z	LP_MODE_OTA1_Z	**RESV**	**RESV**	LP_MODE_OTA2_XY	LP_MODE_OTA1_XY	0x00	R/W

Bit	Name	Function	Description
0	LP_MODE_OTA1_XY	Additional control for OTA1 low power mode.	0: Fs = 1.6 MHz (default). 1: Fs = 200 kHz.
1	LP_MODE_OTA2_XY	Additional control for OTA2 low power mode.	0: Disabled (default) 1: Fs <= 1.6 MHz.
3:2	**RESV**	Reserved.	Reserved.
4	LP_MODE_OTA1_Z	Additional control for OTA1 low power mode.	0: Fs = 1.6 MHz (default). 1: Fs = 200 kHz.
5	LP_MODE_OTA2_Z	Additional control for OTA2 low power mode.	0: Disabled (default) 1: Fs <= 1.6 MHz.
6	PMU_DLDO_STB_BOOST	Boost DLDO regulator bias current in duty cycled, low power mode.	0: Boost current is disabled (default). 1: Boost current is enabled Enabling the 'boost' bits for the ALDO or DLDO will increase current but improve stability.
7	PMU_ALDO_STB_BOOST	Boost ALDO regulator bias current in duty cycled, low power mode.	

Table 6-73: Register 0x8C bit assignments

MEMSIC

6.1.70 0X8D – ANALOG CONTROL REGISTER 6

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x8D	**ANA_CTRL_6 Analog Control Register 6**	**RESV**	**RESV**	INT2_ PE_EN	TEST_INT1_ PE_EN	SPI_ DOUT_ PE_EN	SPI_CS_ PE_EN	SDA_PE _EN	SCL_PE_ EN	0x3F	R/W

Each pad has a weak current pullup to keep undriven or disabled pads from floating or causing high current draw. Each bit defaults to a logic '1' or "enable pullup" following a POR or soft-reset.

Bit	Name	Function	Description
0	SCL_PE_EN	SCL pad pullup-enable.	0: Pad 50nA pullup is not enabled. 1: Pad 50nA pullup is enabled (default).
1	SDA_PE_EN	SDA pad pullup-enable.	0: Pad 50nA pullup is not enabled. 1: Pad 50nA pullup is enabled (default).
2	SPI_CS_PE_EN	CS# pad pullup-enable.	0: Pad 50nA pullup is not enabled. 1: Pad 50nA pullup is enabled (default).
3	SPI_DOUT_PE_EN (SDO_PE_EN)	SDO pad pullup-enable.	0: Pad 50nA pullup is not enabled. 1: Pad 50nA pullup is enabled (default).
4	TEST_INT1_PE_EN	INT1 pad pullup-enable.	0: Pad 50nA pullup is not enabled. 1: Pad 50nA pullup is enabled (default).
5	INT2_PE_EN	INT2 pad pullup-enable.	0: Pad 50nA pullup is not enabled. 1: Pad 50nA pullup is enabled (default).
6	**RESV**	Reserved	Reserved.
7	**RESV**	Reserved	Reserved.

Table 6-74: Register 0x8D bit assignments

6.1.71 0X90 – Z-AXIS DECIMATION COUNT

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x90	XL_DEC_REG_Z XL Z Decimation Register	XL_Z_DEC_CNT_Z[7:0]								0x04	R/W

Bit	Name	Description
7:0	XL_Z_DEC_COUNT[7:0]	Set the decimation count for the XL Z channel; does not apply to X or Y. • The XL Z averaging filter must be enabled for the decimation count to apply (register 0x91 bit 1 = '1'), otherwise the count is set to 1. • If the Z-channel SDM mode is set to "non-overlap, double Z mode" (register 0x91 [3:2] = '01') AND the Z-averaging filter is enabled (register 0x91 bit 1 = '1', the averaging filter decimation count is **divided by 2**. 0x00: Z decimation count is 256 (default). 0x01-0xFF, Z decimation count is 1 to 255. See register 0x91 for additional Z-channel controls. Also see register 0x22, the XY-axis decimation count.

Table 6-75: register 0x90 bit assignments

MEMSIC

6.1.72 0X91 – Z-AXIS CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x91	XL_DEC_REG_Z Z Decimation Register	**RESV**	XL_OSR_SEL_Z[2:0]			XL_SDM_MODE_Z[1:0]		XL_WTD_AVG_FILTER_Z_EN	**RESV**	0x10	R/W

Bit	Name	Function	Description
0	**RESV**	Reserved.	Reserved.
1	XL_WTD_AVG_FILTER_Z_EN	Enable control, Z-axis WAF.	0: Z-axis weighted average filter is disabled (default). 1: Z-axis weighted average filter enabled.
3:2	XL_SDM_MODE_Z[1:0]	Z-channel SDM sampling mode.	Select Z-axis sampling mode; also affects the shared X and Y sampling. 00 Z-axis only 01: Z-axis runs double 10: Z-axis overlap X and Y sampling 11: XY, Z are both switched
6:4	XL_OSR_SEL_Z[2:0]	Z-axis OSR select.	**OSR[2:0]** / **Selected OSR** / **Notes** **000** / 32 / Sinc filter output rate is Fs/32. **001** / 64 / Sinc filter output rate is Fs/64. **010** / 125 / Sinc filter output rate is Fs/128. **011** / 256 / Sinc filter output rate is Fs/256. **100** / 512 / Sinc filter output rate is Fs/512.
7	**RESV**	Reserved.	Reserved.

Table 6-76: Register 0x91 bit assignments

MEMSIC

6.1.73 0X92 – SELF-TEST HOLD COUNT REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x92	RESV	SLFTST_HOLD_CNT[7:0]								0x00	R/W

Bit	Name	Function	Description
7:0	SLFTST_HOLD_CNT[7:0]	Self-test hold count parameter.	The self-test hold count is the number of system clock cycles the MEMS is held in tilt mode during the self-test operation. The actual counter is a 17-bit value. The counter terminal count value is {slftst_hold_cnt[7:0], 000000000}. For example, if the system clock frequency is 1.6 MHz, loading a value of 0x20 in register 0x92 will result in a ~10ms MEMS hold time. {reg92[7:0],000000000} -> {0010_0000,000000000} -> 0x4000 0x4000 -> 16384 decimal 16384 x 625 ns = 10.240 ms MEMS hold time delay

Table 6-77: Register 0x92 bit assignments

MEMS

6.1.74 0X94 – DIGITAL TEST REGISTER 2 (SELF-TEST COUNT)

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x94	**DTEST_REG_2 Digital Test Register 2 (Self-Test Count)**	**RESV**	INT1_EXT_CLK_SEL	SLFTST_CNT[5:0]						0x14	R/W

Bit	Name	Function	Description
5:0	SLFTST_CNT[7:0]	Self-test count parameter.	This 6-bit unsigned value is the number of system/sample clocks to wait before capturing data into the sinc filter. Once the tilt hold count has been reached (reg 0x92), the MEMS is released from the tilt position. The sinc filter will begin capturing data from the SDM/ADC after the count in register 0x94 has been reached. Minimum value: 0x01 Default value: 0x14 (20 cycles) Maximum value: 0x3F (63 cycles)
6	INT1_EXT_CLK_SEL	Enable external system clock injection via the INT1 pad.	0: External clock injection is INT2 pad (default). 1: External clock injection is INT1 pad, and external clock enabled to replace SYS_OSC from analog. Once this bit is 0, INT2 pad works as external clock injection. It still needs to assert Reg93 bit3 to enable external clock to replace SYS_OSC from analog.
7	RESV	Reserved.	Reserved.

Table 6-78: Register 0x94 bit assignments

6.1.75 0X95 – WARM-UP REGISTER (SDM POWER DELAY COUNT)

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x95	**Warm-up Register WARM_UP_REG**	SDM_PWR_DLY_CNT[7:0]								0x08	R/W

Bit	Name	Function	Description
7:0	SDM_PWR_DLY_CNT[7:0]	Warm-up count for SDM, Self-test count parameter.	This 8-bit unsigned value is left shifted by 1 to form the SDM power delay count. This is the time between when the SDM/ADCs are powered up and when sampling begins. In duty-cycled, low power modes the SDM/ADC may be optionally powered off between XYZ samples. This programmable count allows for the SDM/ADC and analog to bias and stabilize. Any non-zero value programmed into this register will be multiplied by 2 to form the actual delay time. For example, if 0x03 is loaded into register 0x95, the SDM_PWR_DLY count will be 0x06 system/ sample clocks. Note that any duty-cycled ODR must take this delay time into account. Minimum value: 0x00 (default) Maximum value: 0xFF (Yields 0x1FE or 510 counts). Maximum delay time at 1.6 MHz is ~318 us

Table 6-79: Register 0x95 bit assignments

6.1.76 0X98 – SINC DUMMY COUNT REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x98	**SINC Dummy Count Register** **DUMMY_CNT_REG**	SINC_DUMMY2_CNT[3:0]				SINC_DUMMY1_CNT[3:0]				0x00	R/W

Bit	Name	Function	Description
3:0	SINC_DUMMY1_CNT[3:0]	Dummy or delay count for SINC filters.	Set the number of clock cycles for the DUMMY1 delay period times 4. 0x0 – Dummy1 count is 0 0x1 – Dummy1 count is 4 0x2 – Dummy1 count is 8 0x3 – Dummy1 count is 12 … 0xF – Dummy1 count is 60 (15 x 4).
7:4	SINC_DUMMY2_CNT[3:0]	Dummy or delay count for SINC filters.	Set the number of clock cycles for the DUMMY2 delay period times 4. 0x0 – Dummy2 count is 0 0x1 – Dummy2 count is 4 0x2 – Dummy2 count is 8 0x3 – Dummy2 count is 12 … 0xF – Dummy2 count is 60 (15 x 4).

Table 6-80: Register 0x98 bit assignments

See register 0x9D for the SINC_STATE_XY and SINC_STATE_Z FSM states. The dummy counts control the DUMMY1 and DUMMY2 state delays.

6.1.77 0X9C – XL SELF-TEST REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x9C	XL_SELF_TEST_2	STICTION_POLARITY_SWAP	D_ZPST_IS_GND_O	SLFTST_TANDR_PM_HIGH	SLFTST_TANDR_N_HIGH	SLFTTST_MAN_EN	SLFTST_TANDR_Z_EN	SLFTST_TANDR_Y_EN	SLFTST_TANDR_X_EN	0x00	R/W

Bit	Name	Function	Description
0	SLFTST_TANDR_X_EN	MEMS self-test, tilt-and-release enable, X-axis.	0: X-axis/MEMS self-test mode is not enabled (default). 1: X-axis/MEMS self-test mode is enabled. Generally self-test is managed by the XL_CTRL state machine. Set register 0x04 bits 1:0 = '10' for self-test mode to be active. If more than one channel is selected for self-test (bits 2:0), the X, Y, and then Z will be given priority. It is required to run self-test one channel at a time. The state machine supports single channel execution only.
1	SLFTST_TANDR_Y_EN	MEMS self-test, tilt-and-release enable, Y-axis.	0: Y-axis/MEMS self-test mode is not enabled (default). 1: Y-axis/MEMS self-test mode is enabled. Generally self-test is managed by the XL_CTRL state machine. Set register 0x04 bits 1:0 = '10' for self-test mode to be active.
2	SLFTST_TANDR_Z_EN	MEMS self-test, tilt-and-release enable, Z-axis.	0: Z-axis/MEMS self-test mode is not enabled (default). 1: Z-axis/MEMS self-test mode is enabled. Generally self-test is managed by the XL_CTRL state machine. Set register 0x04 bits 1:0 = '10' for self-test mode to be active.
3	SLFTTST_MAN_EN	Manual control of self-test feature.	0: XL_CTRL state machine manages self-test mode (default). 1: XL_CTRL state machine does not manage self-test mode, bits 2:0 allow for direct selection of axis enable.
4	SLFTST_TANDR_N_HIGH	Select level of self-test.	0: Self-test level is set to high (default). 1: Self-test level is set to low.
5	SLFTST_TANDR_PM_HIGH	Select level of PM drive during self-test.	0: PM drive high is not enabled during self-test (default). 1: PM drive high is enabled during self-test.
6	D_ZPST_IS_GND_O	Set the level on the ZPST pin.	0: ZPST_IS_GND is set to AVDD (default) 1: ZPST_IS_GND is set to GND (Like original Atria1).
7	STICTION_POLARITY_SWAP	Swap the polarity of the stiction detection level.	Set the polarity of the SLFTST_TANDR_N_HIGH assertion level. 0: SLFTST_TANDR_N_HIGH level = polarity of digital flag (default) 1: SLFTST_TANDR_N_HIGH level = ~polarity of digital flag

Table 6-81: Register 0x9C bit assignments

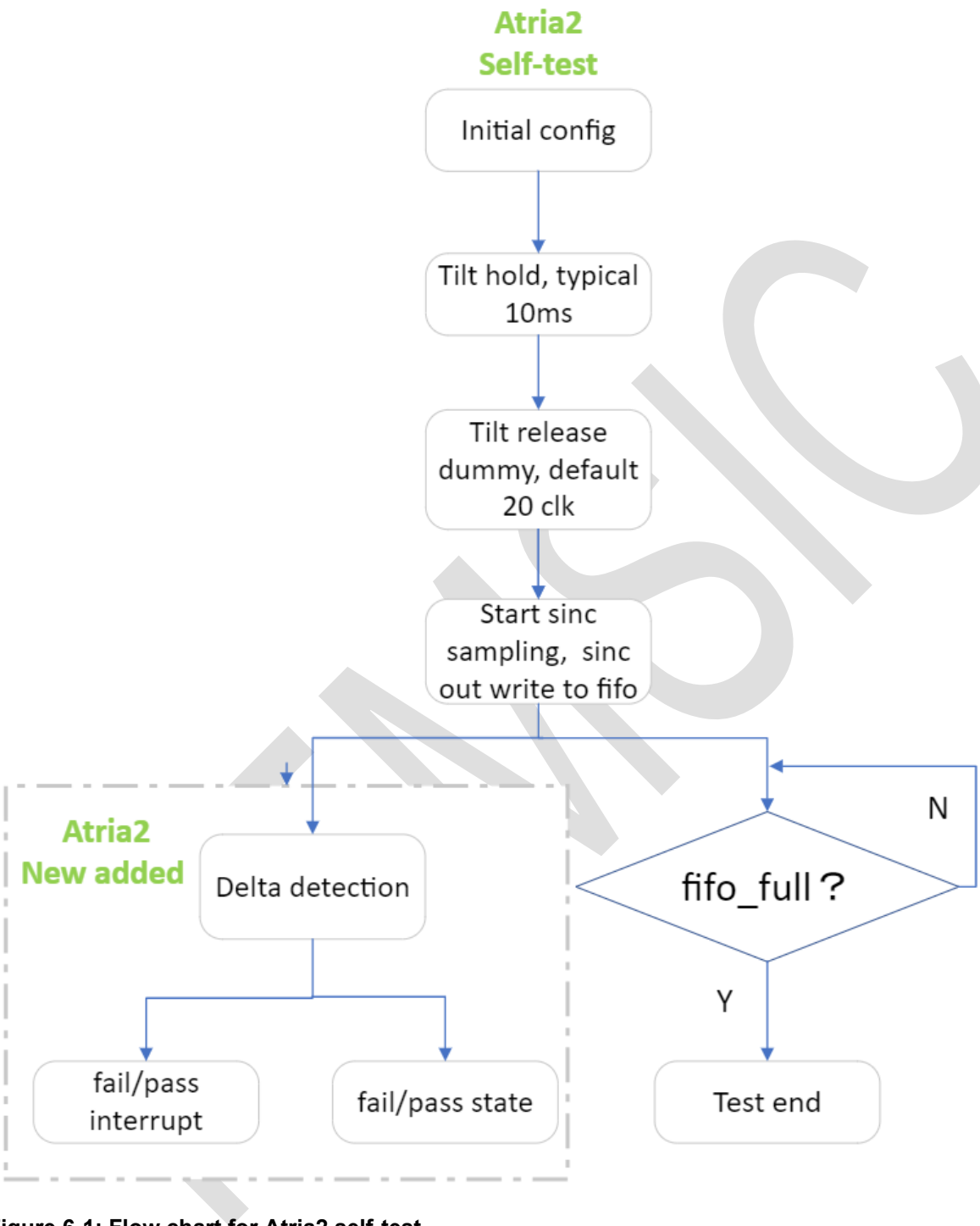


Figure 6-1: Flow chart for Atria2 self-test

6.1.78 0X9D – XL SINC STATE FSM STATUS REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x9D	**XL_SINC_STATE_FSM** **XY and Z SINC FSM Status Register**	MOTION_CURRENT_ST[1:0]		SINC_STATE_Z[2:0]			SINC_STATE_XY[2:0]			0x00	RO

This read-only register reports the current state of the XL SINC state machines, XY and Z.

Bit	Name	Function	Description
2:0	SINC_STATE_XY[2:0]	XL control state machine.	SINC_IDLE = 4'd0, SINC_DUMMY1 = 4'd1, SINC_DUMMY2 = 4'd2, SINC_X = 4'd3, SINC_Y = 4'd4 Other states apply to Z axis only.
5:3	SINC_STATE_Z[2:0]	XL control state machine.	SINC_IDLE = 4'd0, SINC_DUMMY1 = 4'd1, SINC_DUMMY2 = 4'd2, SINC_Z1 = 4'd3, SINC_Z2 = 4'd4, SINC_Z_DLY = 4'd5, SINC_Z3 = 4'd6, SINC_DUMMY3 = 4'd7;

7:6	MOTION_CURRENT_ST[1:0]	Motion interface state machine.	IDLE = 2'b00, // Motion FSM is idle
			X_CH = 2'b01, // X sample sent to motion logic
			Y_CH = 2'b10, // Y sample sent to motion logic
			Z_CH = 2'b11 // Z sample sent to motion logic
			
			Shows the status of the FSM that feeds X, Y, and Z sample data into the motion detection logic.

Table 6-82: Register 0x9D bit assignments

6.1.79 0XA0, 0XA1 – XY AXIS DCM TEST REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0xA0	**XL_DCM_XY_LSB**	XL Duty Cycle XY LSB	XL_DCM_XY[7:0]								0x00	R/W
0xA1	**XL_DCM_XY_MSB**	XL Duty Cycle XY MSB	XL_DCM_XY[15:8]								0x00	R/W

6.1.79.1 DCM/DUTY CYCLE GENERATORS

The duty cycle generator modules (DCM) output a 1-bit waveform that is very similar to the duty-cycle output of the actual AGC/SDM. When the DCM is enabled, the input to the sinc filter is switched from the external SDM/ADC to the internal DCM source.

6.1.79.2 DUTY CYCLE PERCENTAGES

The percentage duty cycle a DCM can generate is related to the OSR selected. The table below shows sample duty cycle percentages for various OSRs. The higher the OSR, the more settings that are available between 0% and 100%. For example, at OSR32 there are 32 possible duty cycle percentages available, at OSR256, there are 256 values available. A 50% duty cycle is 0g.

Note that in Atria2, the highest OSR is 512.

Percentage	OSR 32 Write value to DCM	OSR 64 Write value to DCM	OSR 128 Write value to DCM	OSR 256 Write value to DCM	OSR 512 Write value to DCM	OSR 1024 Write value to DCM	OSR 2048 Write value to DCM	OSR 4096 Write value to DCM	Expected XL RBM Output
0%	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0xC000
25%	0x008	0x0010	0x0020	0x0040	0x0080	0x0100	0x0200	0x0400	0xE000
50%	0x0010	0x0020	0x0040	0x0080	0x0100	0x0200	0x0400	0x0800	0x0000
75%	0x0018	0x0030	0x0060	0x00C0	0x0180	0x0300	0x0600	0x0C00	0x2000
100%	0x0020	0x0040	0x0080	0x0100	0x0200	0x0400	0x0800	0x1000	0x3FFF

Table 6-83: DCM values with OSR

6.1.80 0XA2 – INTERRUPT AUTO CLEAR REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0xA2	**INTR_AUTO_CLR**	Interrupt Auto Clear Register	**RESV**	AUTO_CLEAR_EN	MOTIONLESS_CFG[2:0]			AUTO_CLEAR_CFG[2:0]			0x00	R/W

Bit	Name	Function	Description
2:0	AUTO_CLEAR_CFG[2:0]	Maximum timing window for an ANY_MOTION interrupt to be serviced/cleared. If the ANY_MOTION interrupt is not cleared during this period, hardware will automatically clear the interrupt and the end of the timing window.	0x0, 0x1: duration 320 ms (default) 0x2: duration 640 ms 0x3: duration 1280 ms 0x4: duration 2560 ms 0x5-0x7: duration 5120 ms See register 0x11 bit 2 and register 0x24 bit 2 for the ANY_MOTION_INTR control. See the following page for the 'auto-clear' sequence.
5:3	MOTIONLESS_CFG[2:0]	Timing window following an ANY_MOTION interrupt that is serviced and cleared by software. If no additional ANY_MOTION interrupts are triggered during the timing window, a new MOTIONLESS interrupt will be asserted by hardware.	0x0, 0x1: duration 320 ms (default) 0x2: duration 640 ms 0x3: duration 1280 ms 0x4: duration 2560 ms 0x5-0x7: duration 5120 ms See register 0x11 bit 6 and register 0x25 bit 6 for the MOTIONLESS_INTR control. See the following page for the 'motionless' sequence.
6	AUTO_CLEAR_EN	Enable the auto clear feature for the ANY_MOTION interrupt.	0: AUTO_CLEAR feature is disabled (default). 1: AUTO_CLEAR feature is enabled.
7	**RESV**	Reserved.	Reserved, returns '0' when read.

Table 6-84: Register 0xA2 bit assignments

NEW

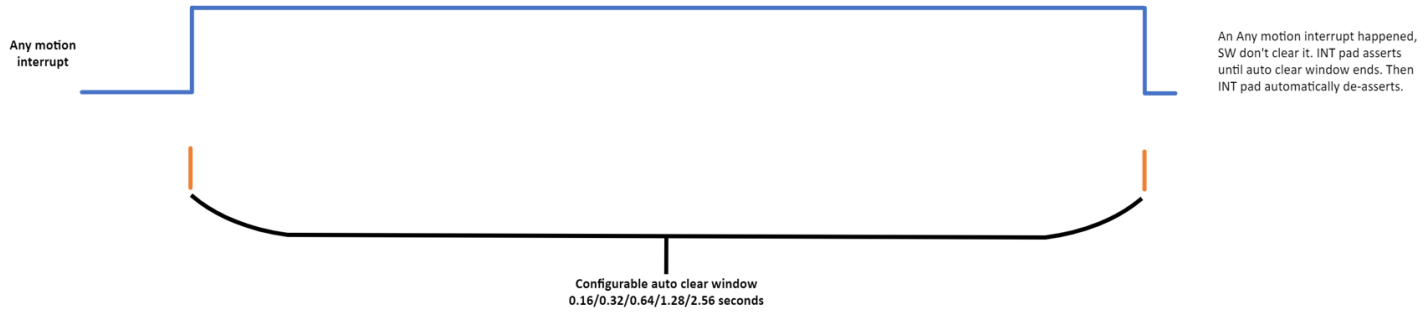


Figure 6-2: AUTO_CLEAR with ANY_MOTION interrupt

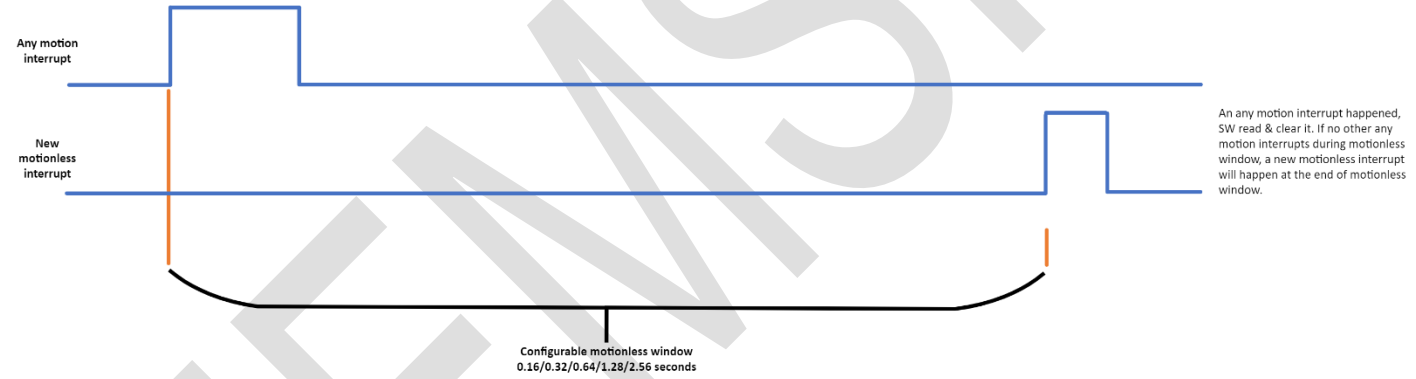


Figure 6-3: MOTIONLESS with ANY_MOTION interrupt

MEMSIC

6.1.81 0XA4,0XA5 –Z AXIS DCM TEST REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0xA4	**XL_DCM_Z_LSB**	XL Duty Cycle X LSB	XL_DCM_Z[7:0]								0x00	R/W
0xA5	**XL_DCM_Z_MSB**	XL Duty Cycle X MSB	XL_DCM_Z[15:8]								0x00	R/W

See registers 0xA0, 0xA1 for a description of the DCM/duty cycle modulator features and usage.

MEMSIC

6.1.82 0XA9,0XAA – TEMPERATURE CALIBRATION OUTPUT REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0xA9	TEMP_CAL_OUT_LSB	Temp Debug Register	DUT_TEMP_OUT[7:0]								0x00	RO
0xAA	TEMP_CAL_OUT_MSB	Temp Debug Register	TCS_OUT[11:8]				RESV	DUT_TEMP_OUT[10:8]			0x00	RO

The output temperature is clamped between 223 and 398 kelvin. The dut_temp_out[10:0] is computed using the following formula in the temp_cal module in hardware

$$\boldsymbol{T} = \frac{\frac{\boldsymbol{code(T0)}}{\boldsymbol{code(T)}} - \mathbf{1}}{\boldsymbol{TC1}} + \boldsymbol{T0} = \boldsymbol{GC1} * \left(\frac{\boldsymbol{code(T0)}}{\boldsymbol{code(T)}} - \mathbf{1} \right) + \boldsymbol{T0}$$

$T0$: calibration temperature

$code(T0)$: temperature sensor output code (11-bit) at calibration temperature $T0$

$code(T)$: temperature sensor output code (11-bit) at temperature T

$TC1$: linear fit coefficient

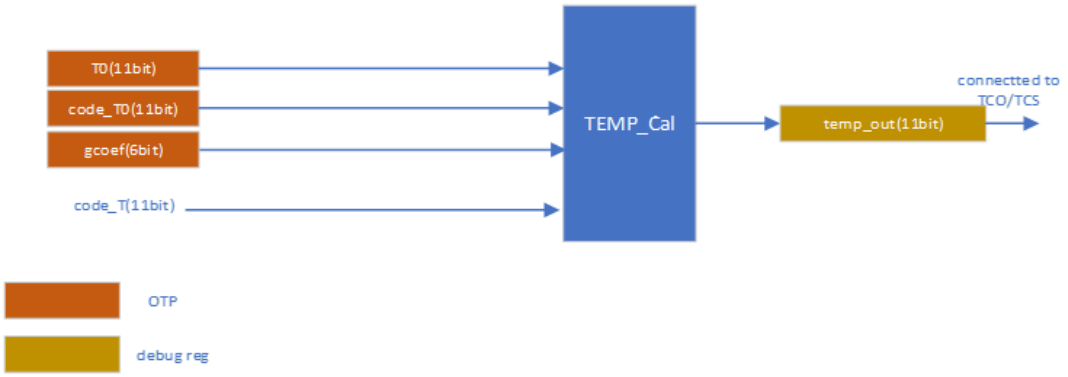
$GC1$: $GTC1 = 1/TC1$ (9-bit)

T: current temperature (11-bit)

Interface	Definition	Range	Width	Registers
code_T0	$code(T0)$, read from OTP	800~1400	11-bits	{Reg7C[7:0], reg7B[5:3]}
temp_T0	$T0$, read from OTP	293~303	11-bits	{Reg7B[2:0], reg7A[7:0]}
gcoef	$GC1$, read from OTP	200-500	9-bits	{Reg7B[6], reg7D[7:0]}

Table 6-85: OTP based temperature trim values

$$T = GC1 * \left(\frac{\mathbf{code(T0)}}{\mathbf{code(T)}} - \mathbf{1} \right) + \mathbf{T0}$$



Interface name	definition	range	width
code_T0	$code(T0)$, read from OTP	800~1400	input [10:0]
temp_T0	$T0$,read from OTP	293~303	input [10:0]
gcoef	$GC1/8$, read from OTP	25~63	input [5:0]
din_data	code(T), sensor output data	0~1023	input [10:0]
din_busy	handshake of input	0/1	output
din_vld	handshake of input	0/1	input
dout_data	T, output data	223-398	output [10:0]
dout_busy	handshake of output	0/1	Input
dout_vld	handshake of output	0/1	Output

Figure 6-4: Temperature calibration block details

6.1.83 0XAB,0XAC – SELF TEST THRESHOLD REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0xAB	**SLFTST_TH_LSB**	Self-Test Threshold LSB	SLFTST_TH[7:0]								0x00	R/W
0xAC	**SLFTST_TH_LSB MSB**	Self-Test Threshold MSB	SLFTST_TH[15:8]								0x00	RW

Bit	Name	Function	Description
0xAB[7:0] **0xAC[8:0]**	SLFTST_TH[15:0]	Self-test threshold setting	The self-test threshold use an unsigned 16-bit delta count for determining the pass/fail status of the TANDR self-test. As the self-test data is being read and captured to the FIFO, the maximum and minimum values from the SINC filter data are stored. Hardware will identify the maximum and minimum signed values. After the self-test is completed, the delta value will be calculated by subtracting the max – min captured values. The delta count is compared with the self-test threshold to determine pass for fail. **SLFTST_RESULT = DELTA > SLFTST_TH** 0x0000 – minimum self-test threshold ….. 0xFFFF – maximum self-test threshold • Competition of the self-test is indicated by register 0x97 bit 7. • Pass/fail status of the self-test is indicated by register 0x12 bit 0. • The self-test interrupt status is located at register 0x10 bit 0.

Table 6-86: Registers 0xAB,0xAC bit assignments

See sections Register 0x04 Self-test mode for more information.

6.1.84 0XAD-0XB4 – Z AXIS LPF COEFFICIENTS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0xAD	Z LPF Coefficient B0 LSB	Z_LPF_B0[7]	Z_LPF_B0[6]	Z_LPF_B0[5]	Z_LPF_B0[4]	Z_LPF_B0[3]	Z_LPF_B0[2]	Z_LPF_B0[1]	Z_LPF_B0[0]	0x00	R/W
0xAE	Z LPF Coefficient B0 MSB	Z_LPF_B0[15]	Z_LPF_B0[14]	Z_LPF_B0[13]	Z_LPF_B0[12]	Z_LPF_B0[11]	Z_LPF_B0[10]	Z_LPF_B0[9]	Z_LPF_B0[8]	0x00	R/W
0xAF	Z LPF Coefficient B1 LSB	Z_LPF_B1[7]	Z_LPF_B1[6]	Z_LPF_B1[5]	Z_LPF_B1[4]	Z_LPF_B1[3]	Z_LPF_B1[2]	Z_LPF_B1[1]	Z_LPF_B1[0]	0x00	R/W
0xB0	Z LPF Coefficient B1 MSB	Z_LPF_B1[15]	Z_LPF_B1[14]	Z_LPF_B1[13]	Z_LPF_B1[12]	Z_LPF_B1[11]	Z_LPF_B1[10]	Z_LPF_B1[9]	Z_LPF_B1[8]	0x00	R/W
0xB1	Z LPF Coefficient A1 LSB	Z_LPF_A1[7]	Z_LPF_A1[6]	Z_LPF_A1[5]	Z_LPF_A1[4]	Z_LPF_A1[3]	Z_LPF_A1[2]	Z_LPF_A1[1]	Z_LPF_A1[0]	0x00	R/W
0xB2	Z LPF Coefficient A1 MSB	Z_LPF_A1[15]	Z_LPF_A1[14]	Z_LPF_A1[13]	Z_LPF_A1[12]	Z_LPF_A1[11]	Z_LPF_A1[10]	Z_LPF_A1[9]	Z_LPF_A1[8]	0x00	R/W
0xB3	Z LPF Coefficient A2 LSB	Z_LPF_A2[7]	Z_LPF_A2[6]	Z_LPF_A2[5]	Z_LPF_A2[4]	Z_LPF_A2[3]	Z_LPF_A2[2]	Z_LPF_A2[1]	Z_LPF_A2[0]	0x00	R/W
0xB4	Z LPF Coefficient A2 MSB	Z_LPF_A2[15]	Z_LPF_A2[14]	Z_LPF_A2[13]	Z_LPF_A2[12]	Z_LPF_A2[11]	Z_LPF_A2[10]	Z_LPF_A2[9]	Z_LPF_A2[8]	0x00	R/W

Bit	Name	Function	Description
0xAD 7:0 **0xAE 7:0**	Z LPF Coefficient B0/B2 LSB/MSB	16-bit value for LPF coefficient B0 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0xAF 7:0 **0xB0 7:0**	Z LPF Coefficient B1 LSB/MSB	16-bit value for LPF coefficient B1 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0xB1 7:0 **0xB2 7:0**	Z LPF Coefficient A1 LSB/MSB	16-bit value for LPF coefficient A1 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements. *This value is always considered a negative coefficient by the filter hardware.*
0xB3 7:0 **0xB4 7:0**	Z LPF Coefficient A2 LSB/MSB	16-bit value for LPF coefficient A2 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.

Table 6-87: Registers 0xAD-0xB4 bit assignments

7 LIST OF TABLES

Table 1: Order Information 6
Table 2: Package Information 6
Table 3: Pin Description 10
Table 4: Absolute Maximum Ratings 18
Table 5: Accel Sensor Characteristics 19
Table 6: Electrical Characteristics 20
Table 7: SPI Timing Parameters 23
Table 8: I2C Address Selection 24
Table 9: I2C Timing Characteristics 24
Table 10: I3C Timing Parameters 26
Table 11: I2C Address Selection 28
Table 12: Operating Modes 29
Table 6-1: Register Pg0 0x02 bit assignments 31
Table 6-2: Register 0x03 assignments 32
Table 6-3: Register 0x04 assignments 33
Table 6-4: Self-test basic operation 36
Table 6-5: Register 0x05 assignments 38
Table 6-6: Power Modes 39
Table 6-7: Power modes vs SINC/SDM sampling modes 39
Table 6-8: Register 0x06 assignments 41
Table 6-9: Register 0x07 assignments 42
Table 6-10: Register 0x10 bit assignments 46
Table 6-11: Register 0x11 bit assignments 46
Table 6-12: register 0x12 bit assignments 47
Table 6-13: register 0x13 bit assignments 48
Table 6-14: register 0x14 bit assignments 49
Table 6-15: register 0x15 bit assignments 50
Table 6-16: register 0x16 bit assignments 51
Table 6-17: register 0x17 bit assignments 52
Table 6-18: register 0x18 bit assignments 53
Table 6-19: registers 0x19-0x1E bit assignments 54
Table 6-20: register 0x1F bit assignments 55

MEMSIC

Table 6-21: register 0x20 bit assignments 56
Table 6-22: register 0x21 bit assignments 57
Table 6-23: register 0x22 bit assignments 58
Table 6-24: Register 0x23 bit assignments 59
Table 6-25: Register 0x24 bit assignments 60
Table 6-26: Register 0x25 bit assignments 61
Table 6-27: Register 0x26 bit assignments 62
Table 6-28: Register 0x27 bit assignments 64
Table 6-29: Register 0x28 bit assignments 65
Table 6-30: Register 0x29 bit assignments 66
Table 6-31: Register 0x2A bit assignments 67
Table 6-32: Register 0x2B, 0x2C bit assignments 68
Table 6-33: Register 0x2D bit assignments 69
Table 6-34: Register 0x2E bit assignments 70
Table 6-35: Register 0x2F bit assignments 71
Table 6-36: Register 0x30 bit assignments 72
Table 6-37: Registers 0x31,0x32 bit assignments 73
Table 6-38: Register 0x33 bit assignments 74
Table 6-39: Register 0x34,0x35 bit assignments 75
Table 6-40: Register 0x2A,0x2B bit assignments 79
Table 6-41: Register 0x3D bit assignments 80
Table 6-42: Register 0x3E bit assignments 81
Table 6-43: Register 0x3F bit assignments 82
Table 6-44: Register 0x40 bit assignments 83
Table 6-45: Register 0x41,0x42 bit assignments 84
Table 6-46: Register 0x43 bit assignments 85
Table 6-47: Register 0x44,0x45 bit assignments 86
Table 6-48: Register 0x46,0x47 bit assignments 87
Table 6-49: Register 0x48 bit assignments 88
Table 6-50: Register 0x49 bit assignments 89
Table 6-51: Register 0x4A bit assignments 90
Table 6-52: Registers 0x4E-0x55 bit assignments 91
Table 6-53: Register 0x56 bit assignments 92
Table 6-54: Register 0x58-0x5D bit assignments 93

MEMSIC

Table 6-55: Register 0x5E-0x61,0x6C,0x79 bit assignments 94
Table 6-56: Register 0x62 bit assignments 95
Table 6-57: Register 0x63-0x69 bit assignments 96
Table 6-58: Register 0x6A bit assignments 97
Table 6-59: Register 0x6B bit assignments 98
Table 6-60: MEMS sensitivity vs analog gain 99
Table 6-61: TCO coefficients 100
Table 6-62: Format and range of TCO coefficients 100
Table 6-63: Format for X-axis gain shift 101
Table 6-64: TCS coefficients 102
Table 6-65: Format and range of TCS coefficients 103
Table 6-66: Y and z gain shift assignments 104
Table 6-67: Registers 0x7A,0x7B,0x7C,0x7D bit assignments 105
Table 6-68: Registers 0x69,0x7E,0x7F,0x80 bit assignments 107
Table 6-69: Register 0x81 bit assignments 108
Table 6-70: Register 0x82 bit assignments 108
Table 6-71: Register 0x84-0x87 suggested assignments 109
Table 6-72: Register 0x88 bit assignments 110
Table 6-73: Register 0x8C bit assignments 111
Table 6-74: Register 0x8D bit assignments 112
Table 6-75: register 0x90 bit assignments 113
Table 6-76: Register 0x91 bit assignments 114
Table 6-77: Register 0x92 bit assignments 115
Table 6-78: Register 0x94 bit assignments 116
Table 6-79: Register 0x95 bit assignments 117
Table 6-80: Register 0x98 bit assignments 118
Table 6-81: Register 0x9C bit assignments 119
Table 6-82: Register 0x9D bit assignments 121
Table 6-83: DCM values with OSR 122
Table 6-84: Register 0xA2 bit assignments 123
Table 6-85: OTP based temperature trim values 126
Table 6-86: Registers 0xAB,0xAC bit assignments 128
Table 6-87: Registers 0xAD-0xB4 bit assignments 129

MEMSIC

8 LIST OF FIGURES

Figure 1: Block Diagram 7
Figure 2: Package Outline and Mechanical Dimensions 8
Figure 3: Package Orientation 9
Figure 4: Package Axis Reference 9
Figure 5: Typical I2C Application Circuit 11
Figure 6: Typical I3C Application Circuit 12
Figure 7: Typical 4-wire SPI Application Circuit 13
Figure 8: Typical 3-wire SPI Application Circuit 14
Figure 9: Tape Dimensions 15
Figure 10: Reel Dimensions 16
Figure 11: SPI single register write cycle 21
Figure 12: SPI Burst register write cycle (2 registers) 22
Figure 13: SPI single register read cycle 22
Figure 14: SPI Burst register read cycle (2 registers) 22
Figure 15: SPI Timing Waveform 23
Figure 16. I2C Interface Timing 24
Figure 17: I3C START Condition Timing 27
Figure 18: I3C STOP Condition Timing 27
Figure 19: I3C Target Out Timing 27
Figure 6-1: Flow chart for Atria2 self-test 120
Figure 6-2: AUTO_CLEAR with ANY_MOTION interrupt 124
Figure 6-3: MOTIONLESS with ANY_MOTION interrupt 124
Figure 6-4: Temperature calibration block details 127

MEMSIC

9 REVISION HISTORY

Date	Revision	Description
2026/04/13	V1.0	Release version 1.0.

MEMSIC

10 LEGAL

1. MEMSIC reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and to this document at any time and discontinue any product without notice. The information contained in this document has been carefully checked and is believed to be accurate. However, MEMSIC shall assume no responsibilities for inaccuracies and make no commitment to update or to keep current the information contained in this document.

2. MEMSIC products are designed only for commercial and normal industrial applications and are not suitable for other purposes, such as: medical life support equipment; nuclear facilities; critical care equipment; military / aerospace; automotive; security or any other applications, the failure of which could lead to death, personal injury or environmental or property damage. Use of the products in unsuitable applications are at the customer's own risk and expense.

3. MEMSIC shall assume no liability for incidental, consequential or special damages or injury that may result from misapplication or improper use of operation of the product.

4. No license, express or implied, by estoppel or otherwise, to any intellectual property rights of MEMSIC or any third party is granted under this document.

5. MEMSIC makes no warranty or representation of non-infringement of intellectual property rights of any third party with respect to the products. MEMSIC specifically excludes any liability to the customers or any third party regarding infringement of any intellectual property rights, including the patent, copyright, trademark or trade secret rights of any third party, relating to any combination, machine, or process in which the MEMSIC products are used.

6. Examples of use described herein are provided solely to guide use of MEMSIC products and merely indicate targeted characteristics, performance, and applications of products. MEMSIC shall assume no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.

7. Information described in this document including parameters, application circuits and its constants and calculation formulas, programs and control procedures are provided for the purpose of explaining typical operation and usage. "Typical" parameters that may be provided in MEMSIC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals," must be validated for each customer application by customer's technical experts. In no event shall the information described be regarded as a guarantee of conditions or characteristics of the products. Therefore, the customer should evaluate the design sufficiently as whole system under the consideration of various external or environmental conditions and determine their application at the customer's own risk. MEMSIC shall assume no responsibility or liability for claims, damages, costs, and expenses caused by the customer or any third party, owing to the use of the above information.

MEMSIC