MEMS-Based System Solutions: Packaging

**Introduction**

The packaging for a MEMS device is a critical component element of delivering a successful MEMS-based system solution (MBSS) to the market as stated in a previous article [1]. Roger Grace Associates’ (RGA) research has found that in typical current MEMS-based products, the packaging cost can be from 20% to 40% of the total material and assembly cost of the product. Testing after packaging is much more costly than testing at the device level because of yield factors. In order to achieve the optimum solution from a yield and cost perspective, testing needs to be conducted at several points of the production process starting with mechanical and electrical testing at the wafer level even before the chip is placed in a package. Additionally, it is crucial that the package is correctly selected/designed for the application. Also, testing can add an additional 20% to 30% to the total cost of the product. It is interesting to note that RGA research established that MEMS suppliers consider packaging to be a major product differentiator and a competitive advantage for their product in the market.

Packaging has a critical role in the commercialisation of MEMS devices and its parameters should be one of the first things to be addressed when developing a MEMS device. Since the package is often the bottle neck to system performance, it needs to be incorporated in the design process, and with the electronics, considered as part of the system. A systems approach where the MEMS, the ASIC and the package are designed simultaneously allows for better partitioning decisions. Subsequently, the system interfaces and design specifications are detailed better and the process lends itself toward better chances of success.

The package design for a MEMS device has to accomplish three objectives: 1) support application-specific operating requirements, 2) prevent degradation of the device performance, and 3) have a manufacturable solution. By nature of being a sensor, and unlike integrated circuits, MEMS devices are subject to additional operating requirements including exposure to media, shock, vibration, extreme temperature, moisture and EMI/RFI. These additional requirements mean that non-standard features need to be added to the package such as a cavity, hole in substrate, optical windows or vacuum hermeticity. Using standard low-cost packaging materials becomes a very challenging scenario when comprehending the potential of final performance and test. The complexity of this situation and the design trade-offs that are implied require that a MEMS concept will need to embody full understanding of all of the constituents of the solution and the specific application at the beginning of the commercialisation process in order to be successful.
MEMS were one of the early examples of SOC (system-on-chip) a.k.a. monolithic as integrated MEMS made in CMOS processes combined one or more MEMS devices, and analog and digital processing on a single chip (figure 1). MEMS products also make use of SIP (System-in-Package) techniques integrating two or more chips in the same package as discussed previously (figure 2). Wire-bonding was used to connect chips in a package for the first MEMS systems and currently this technique is being supplanted by flip chip bonding techniques taken from the IC industry. MEMS products also may be constructed from multiple wafers bonded together. Known as wafer-level packaging (WLP), this technique is driven by the desire to use wafers of different materials, processed by different MEMS fabrication techniques (figure 3). Currently, there is no market driver to standardise packaging (except when IC packages can be used) as companies see proprietary packaging technology as a competitive advantage.

Co-Design
Previously, designers often left design of packaging to the last moment after key sensor and circuit designs had been made. However, this trend is changing as time to market pressure and competition has forced designers to alter their design methodology as market windows were missed due to poorly functioning packages. Lack of design tools has caused package over-designs or package failures as stress and other effects were not properly estimated. New tools for co-design of package, electronics and MEMS devices are enabling better package designs. Many of the delays in bringing MEMS-based systems to market stem from errors made in the design of packaging caused by package-device interactions. Because the package is often a part of the device function, MEMS device performance can often not be predicted until the packaging is completed and all too often, package design is begun after important device design decisions have already been made. For example, quality factor prediction is dependent on package vacuum level and package cavity dimensions. A major design challenge is verification of the package performance and the analysis of the 3D mechanical, thermal and electrical interactions between the package and the individual components.

When the packaging is designed concurrently with the electronics and MEMS components, using co-design tools produces superior system performance results. MEMS and electronics designers can collaborate with package designers to optimise the entire system and trade-off requirements. Co-design

<< Figure 3: Wafer level packaging is gaining great interest in both the IC and MEMS communities. Its use can reduce package size to zero a.k.a. the 'no package' package, provide hermeticity and reduced cost. The sequence of cross section views shows the 3D process for creating a package with high level hermically by sealing a glass wafer to the substrate wafer using anodic bonding, getters and through-glass vias. Courtesy: CEA-Leti (Ref.3) >>

<< Figure 4: Development package services are a critical element in the successful commercialization of MEMS. The ability to convert the results of the front end process i.e. Silicon wafers into usable and measureable devices requires packaging. The ability of a provider of packaging, assembly and testing 'under one roof' accelerates time to market and reduces development costs. The development packaging house acts as the bridge from the wafer fab to the large scale packaging houses. Courtesy: Smart Center. >>

<< Figure 5: SMART Center, Production Packaging and Test Houses >>

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tools enable designers to incorporate the analysis of packaging effects into the component designs enabling overall system performance to be more accurately predicted. For example, device performance degradation due to package stress as a result of the differential expansion of various packaging materials due to TCE (temperature coefficient of expansion) can be calculated and mitigated. Calculating the resonant frequencies of each added component of the packaging is also important, for moving MEMS structures so that exciting unwanted resonant modes is avoided. Co-design also reduces time to market for new products because composition errors can be caught earlier in the design cycle.

**Packaging Development Process: a New Approach**

Billions of dollars have been invested in Silicon fabrication centres at universities and private organisations over the last few decades and it is not uncommon for companies developing MEMS devices to rely on these state-of-the-art fabs for their development work. Resources for MEMS packaging, assembly and testing are equally important but this area has lagged behind because of the 'un glamourous' nature of packaging. The Richard Desich SMART Commercialization Center for Microsystems is a new development resource that provides facilities and expertise to address the challenges of MEMS packaging, assembly and testing for companies looking to develop MEMS products. Access to a commercial development foundry allows companies to acquire actionable information in terms of design, process and calibration to move their projects forward with less cost and risk. A development foundry assists companies that do not have the resources for capital-intensive infrastructure required for MEMS packaging, assembly and testing. Fabless companies have emerged over the years and have been successful in bringing new products to the market. Relying on outsourced manufacturer for development is challenging because it is disruptive to the manufacturer's operations and management of intellectual property can be complicated. An engagement model that offers full access to capabilities required for back-end-of-line process development protects the customers' intellectual property, and with partnerships, assists with the transfer to manufacturing which helps companies get new MEMS products to the market.

The semiconductor supply chain is fragmented and the manufacturing models are driven by high volumes. These two characteristics can make it very difficult for a company interested in developing and launching a new MEMS product. In this case, additional resources are necessary to either manage the suppliers or build a prototype lab. This ultimately detracts from what the company is trying to accomplish — create a new product. The Richard Desich SMART Center offers MEMS developmental packaging and testing services in one location, reducing project costs and accelerating time to market and provides a 'bridge' from the back of the front end (wafer processing) to the beginning of the back end (packaging and testing) for prototype and small volume applications (figure 4). For example, a customer can have their device packaged, performance tested and evaluated for reliability — all at a single facility. Therefore the customer can very quickly understand how their device performs within the constraints of a given package design and its manufacturing process.

**New Developments**

Micro machined inertial sensors have exploded in the consumer and automotive markets and now sell for $1 or less per unit. Tactical and navigation grade (non-MEMS) sensors however require several orders of magnitude better performance and need to function over large temperature ranges and high vibration and shock environments for military, space and industrial applications. These sensors can sell for $1000s per unit — and have the potential to enable a wide range of new commercial and military applications if/when MEMS technologies shrink their size, weight, power and cost of manufacturing. The biggest technical barrier however is the inherent temperature and vibration sensitivity of MEMS devices. Figure 5 shows the environment resistant package (ERP) technology which looks to reduce the environmental sensitivity of these MEMS sensors. As illustrated, it consists of an isolation platform which is optimised either for oven control or vibration filtering. For oven control, the device is thermally isolated from the environment so that it can be heated to a constant temperature with integrated heaters and temperature sensors integrated onto the platform. This is done with a low input power of <50 mW (as compared to typical electronic ovens which consume ~2W or more). For vibration filtering this platform is optimised for filtering high frequency vibration which can be particularly detrimental for gyroscopes. As illustrated, bare dies or fully packaged dies with electronics can be integrated into this isolation platform inside of a ceramic package.

New techniques for packaging have come out of advances in MEMS device fabrication. Through silicon-vias (TSV) are the results of techniques for etching all the way through a wafer for a depth of up to 100s of microns. As a result, MEMS wafer fab supply chains become more prominent. TSVs enable another important packaging technique: that of chip stacking whereby multiple chips are stacked together inside a package and connected together with TSVs. Chip stacking creates a smaller packaging footprint. The design of such a package is more complex as there are thermal dissipation issues as heat must be removed between the chips stacked in close proximity and the mechanical stability must be carefully simulated to ensure good performance and reliability. Traditional IC packaging houses are also beginning to offer
MEMS specific packages and equipment vendors are jumping in to supply new packaging and testing equipment. Hence, the packaging options for MEMS devices are numerous and the trend of MEMS incorporating multiple sensors along with associated software to create higher added value systems is converging with the availability of new multi-chip packaging solutions. Chip stacking can be realised in a one-at-a-time fashion or through wafer level packaging (WLP) approach addressed earlier.

Another approach to novel packaging is the ‘no package’ package. To address the demands of extremely small size and low cost demanded by the consumer electronics to market, a novel packaging techniques using WLP capping wafer and bump bonding to attach the resulting package to the circuit board has been developed by MEMSIC for their MEMS accelerometer (figure 6).

Conclusions/Future Directions
Standardisation of packages will most likely occur as companies focus on other value-add as was done in the IC industry, but this trend will take time. Where packaging is done and by whom will also evolve over time as MEMS and semiconductor fabs and traditional packaging houses compete to supply the newest and highest performance packages and as more traditional semiconductor foundries offer services to the MEMS community. We believe that the ‘no package’ package, which is based on chip stacking/capping will become a very popular approach to provide ultra-miniature and low-cost MEMS-based solutions to the demanding consumer applications sectors including mobile phones and tablets which have recently created a significant double digit growth for the MEMS industry.

It is interesting to note that through substrate vias started with the development of the Silicon Capacitive Pressure Sensors (SCAP) product at Ford in the early 80’s using laser drilling of glass. 30 years later, we are experiencing that this MEMS-based packaging techniques is having a significant impact on the MEMS industry as well as in the IC industry, where it is estimated that in the not too distant future more MEMS wafers will be used for IC device packaging than for MEMS products. Organisations including CEA-Leti are leading the way for the development of both advanced IC and MEMS-based WLP solutions.

Want to Learn More?
Roger Grace will be making a presentation at the Nano-Micro Manufacturing Workshop to take place at Dearborn, Michigan, USA, on 22-23 May 2013 and will provide additional information on several of the topics addressed in this article. To find out more go to www.nano-microworkshop.org.

References
